Atomic Layer Deposition of High-k Dielectric Constant Mixed Oxides and Selective
Atomic Layer Deposition of HfO$_2$ and TiO$_2$ using Metal Organic Precursors and H$_2$O

BY
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THESIS
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1. INTRODUCTION

1.1. Invention of Transistor

Physicist Julius Edgar Lilienfeld filed the first patent for a transistor in Canada in 1925, describing a device similar to a Field Effect Transistor or "FET" [1]. However, Lilienfeld did not publish any research articles about his devices, nor did his patent cite any examples of devices actually constructed. In 1934, German inventor Oskar Heil patented a similar device [2]. From 1942 Herbert Mataré experimented with so-called Duodiodes while working on a detector for a Doppler RADAR system. The dual diodes built by him had two separate but very close metal contacts on the semiconductor substrate. He discovered effects that could not be explained by two independently operating diodes and thus formed the basic idea for the later point contact transistor. In 1947, John Bardeen and Walter Brattain at AT&T's Bell Labs in the United States observed that when electrical contacts were applied to a crystal of germanium, the output power was larger than the input. Solid State Physics Group leader William Shockley saw the potential in this, and over the next few months worked to greatly expand the knowledge of semiconductors. The term transistor was coined by John R. Pierce [3]. According to physicist/historian Robert Arns, legal papers from the Bell Labs patent show that William Shockley and Gerald Pearson had built operational versions from Lilienfeld's patents, yet they never referenced this work in any of their later research papers or historical articles. The transistor is the key active component in practically all modern electronics, and is considered by many to be one of the greatest inventions of the twentieth century [4]. Its importance in today's society rests on its ability to be mass
produced using a highly automated process (semiconductor device fabrication) that achieves astonishingly low per-transistor costs.

Although several companies each produce over a billion individually packaged (known as discrete) transistors every year, the vast majority of transistors now produced are in integrated circuits (often shortened to IC, microchips or simply chips), along with diodes, resistors, capacitors and other electronic components, to produce complete electronic circuits. A logic gate consists of up to about twenty transistors whereas an advanced microprocessor, as of 2009, can use as many as 2.3 billion transistors (MOSFETs). About 60 million transistors were built the year 2002 (figure 3) and the number was potentially increased every year. The transistor's low cost, flexibility, and reliability have made it an ubiquitous device. Transistorized mechatronic circuits have replaced electromechanical devices in controlling appliances and machinery. It is often easier and cheaper to use a standard microcontroller and write a computer program to carry out a control function than to design an equivalent mechanical control function.

1.2. Metal Oxide Semiconductor Field Effect Transistor

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a device used for amplifying or switching electronic signals. The basic principle of the device was first proposed by Julius Edgar Lilienfeld in 1925. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type (see article on semiconductor devices), and is accordingly called an nMOSFET or a pMOSFET (also
commonly nMOS, pMOS). It is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common. The 'metal' in the name is now often a misnomer because the previously metal gate material is now often a layer of polysilicon (polycrystalline silicon). Aluminum had been the gate material until the mid 1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates.

A traditional metal–oxide–semiconductor (MOS) structure (figure 1) is obtained by growing a layer of silicon dioxide (SiO₂) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.
Figure 1. A typical scheme of N-type MOSFET
When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If I consider a P-type semiconductor (with $N_A$ the density of acceptors, $p$ the density of holes; $p = N_A$ in neutral bulk), a positive voltage, $V_g$, from gate to body (figure 2) creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If $V_g$ is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator. Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage.
Figure 2. Scheme of MOS Capacitor on P-type Silicon
A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a '+' sign after the type of doping. If the MOSFET is an n-channel or nMOS FET, then the source and drain are 'n+' regions and the body is a 'p' region. As described above, with sufficient gate voltage, holes from the body are driven away from the gate, forming an inversion layer or n-channel at the interface between the p region and the oxide. This conducting channel extends between the source and the drain, and current is conducted through it when a voltage is applied between source and drain. For gate voltages below the threshold value, the channel is lightly populated, and only a very small subthreshold leakage current can flow between the source and the drain.

If the MOSFET is a p-channel or pMOS FET, then the source and drain are 'p+' regions and the body is a 'n' region. When a negative gate-source voltage (positive source-gate) is applied, it creates a p-channel at the surface of the n region, analogous to
the n-channel case, but with opposite polarities of charges and voltages. When a voltage less negative than the threshold value (a negative voltage for p-channel) is applied between gate and source, the channel disappears and only a very small subthreshold current can flow between the source and the drain.

1.3. **Moore’s Law and Transistor Scaling**

Moore's law describes a long-term trend in the history of computing hardware. The number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years [5]. The trend (figure 3) has continued for more than half a century and is not expected to stop until 2015 or later. The capabilities of many digital electronic devices are strongly linked to Moore's law: processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras [6]. All of these are improving at roughly exponential rates as well. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy. Moore's law describes a driving force of technological and social change in the late 20th and early 21st centuries. The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper [8]. The paper noted that number of components in integrated circuits had doubled every year from the invention of the integrated circuit in 1958 until 1965 and predicted that the trend would continue "for at least ten years". His prediction has proved to be uncannily accurate, in part because the law is now used in the semiconductor industry to guide long-term planning and to set targets for research and development [9]. This fact would support the view that the "law"
unfolds as a self-fulfilling prophecy, where the goal set by the prediction charts the course for realized capability.
Figure 3. Diagram of Moore’s Law-predict of the number of transistors integrated per unit circuit area [10]
The basic idea of transistor scaling is to reduce all the dimensions of transistor by a factor k, in addition to the dimensions decreasing; a number of other parameters must increase or decrease.
Table I. Parameters’ change with transistor scaling factor $k$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Constant F Scaling</th>
<th>Generalized Scaling</th>
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<tr>
<td>Device dimension ($L_g$, $W_x$, $T_{ox}$)</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>$k$</td>
<td>$\alpha \cdot k$</td>
</tr>
<tr>
<td>Voltage</td>
<td>$1/k$</td>
<td>$\alpha \cdot k$</td>
</tr>
<tr>
<td>Electric Field (F)</td>
<td>$1$</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Carrier Velocity (v)</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>Depletion layer width (Wd)</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Capacitance ($C = \varepsilon A/t_{ox}$)</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Current (I)</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Circuit delay time ($\tau - C\cdot V/I$)</td>
<td>$1/k$</td>
<td>$1/k$</td>
</tr>
<tr>
<td>Power dissipation per circuit (P-VI)</td>
<td>$1/k^2$</td>
<td>$\alpha /k$</td>
</tr>
<tr>
<td>Power-delay product per circuit (P $\tau$)</td>
<td>$1/k^2$</td>
<td>$\alpha /k$</td>
</tr>
<tr>
<td>Circuit density (-1/A)</td>
<td>$k^2$</td>
<td>$k^2$</td>
</tr>
<tr>
<td>Power density (P/A)</td>
<td>$1$</td>
<td>$\alpha^2$</td>
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</table>
Short channel effects such as DIBL start to occur when the non-scaling of certain parameters such as VT and depletion width occur for the shortest gate-length transistors. Constant electric field scaling has historically been used as this provides constant power density (the maximum power density is predominantly related to the thermal conductivity of the substrate).

Following figure is shown the result of scaling with the exponential performance improvement of microprocessors and supercomputers since the 1970s. The number of FLOPS is directly related to the number of transistors, the circuit clock speed and the transistor dimensions. Scaling has been occurring since the discovery of the transistor and you can argue that it even goes back to the start of the vacuum tube in the 19th century for all of electronics!
Figure 4. Transistor scaling based on Moore’s law [10]
1.4. **High k dielectric constant materials**

The term high-\(k\) dielectric refers to a material with a high dielectric constant \(k\) (as compared to silicon dioxide) used in semiconductor manufacturing processes which replaces the silicon dioxide gate dielectric. The implementation of high-\(k\) gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law.

Silicon dioxide has been used as a gate oxide material for decades. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current and device performance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to unwieldy power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-\(k\) material allows increased gate capacitance without the concomitant leakage effects.

The gate oxide in a MOSFET can be modeled as a parallel plate capacitor. Ignoring quantum mechanical and depletion effects from the Si substrate and gate, the capacitance \(C\) of this parallel plate capacitor is given by

\[
C = k\varepsilon_0 A/t
\]

(1.1)

Where \(A\) is the capacitor area; \(k\) is the dielectric constant of the gate oxide material (3.9 for SiO\(_2\)); \(\varepsilon_0\) is permeability of vacuum; \(t\) is the thickness of gate oxide. Since leakage limitation constrains further reduction of \(t\), an alternative method to increase gate capacitance is altering \(k\) by replacing silicon dioxide with a high-\(k\) material.
In such a scenario, a thicker gate layer might be used which can reduce the leakage current flowing through the structure as well as improving the gate dielectric reliability.

The drive current ID for a MOSFET can be written (using the gradual channel approximation) as

\[ I_{D,\text{eff}} = \frac{W}{L} \mu C_{\text{inv}} \left( V_G - V_{th} \right)^2 / 2 \]  

(1.2)

Where, W is the width of the transistor channel; L is the channel length; \( \mu \) is the channel carrier mobility (assumed constant here); \( C_{\text{inv}} \) is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state; \( V_G \) is the voltage applied to the transistor gate; \( V_D \) is the voltage applied to the transistor drain; \( V_{th} \) is the threshold voltage.

The term \( V_G - V_{th} \) is limited in range due to reliability and room temperature operation constraints, since a too large \( V_G \) would create an undesirable, high electric field across the oxide. Furthermore, \( V_{th} \) cannot easily be reduced below about 200 mV [11, 12], because leakage currents due to increased oxide leakage (that is, assuming high-\( \kappa \) dielectrics are not available) and subthreshold conduction raise stand-by power consumption to unacceptable levels. Thus, according to this simplified list of factors, an increased ID, requires a reduction in the channel length or an increase in the gate dielectric capacitance.

1.5. Revolution of Adoption High-\( \kappa \) & Metal Gate
Replacing the silicon dioxide gate dielectric with another material adds complexity to the manufacturing process. Silicon dioxide can be formed by oxidizing the underlying silicon, ensuring a uniform, conformal oxide and high interface quality. As a consequence, development efforts have focused on finding a material with a requisitely high dielectric constant that can be easily integrated into a manufacturing process. Other key considerations include band alignment to silicon (which may alter leakage current), film morphology, thermal stability, maintenance of a high mobility of charge carriers in the channel and minimization of electrical defects in the film/interface. Materials which have received considerable attention are hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide, typically deposited using atomic layer deposition.

It is expected that defect states in the high-k dielectric can influence its electrical properties. Defect states can be measured for example by using zero-bias thermally stimulated current, zero-temperature-gradient zero-bias thermally stimulated current spectroscopy \cite{13,14}, or inelastic electron tunneling spectroscopy (IETS). The industry has employed oxynitride gate dielectrics since the 1990s, wherein a conventionally formed silicon oxide dielectric is infused with a small amount of nitrogen. The nitride content subtly raises the dielectric constant and is thought to offer other advantages, such as resistance against dopant diffusion through the gate dielectric.

In early 2007, Intel announced the deployment of hafnium-based high-k dielectrics in conjunction with a metallic gate for components built on 45 nanometer technologies, and has shipped it in the 2007 processor series codenamed Penryn \cite{10,15}.
At the same time, IBM announced plans to transition to high-k materials, also hafnium-based, for some products in 2008. While not identified, it is most likely the dielectrics used by these companies are some form of nitride hafnium silicates (HfSiON). HfO₂ and HfSiOₓ are susceptible to crystallization during dopant activation annealing. NEC Electronics has also announced the use of a HfSiON dielectric in their 55 nm Ultimate Low Power technology. However, even HfSiON is susceptible to trap-related leakage currents, which tend to increase with stress over device lifetime. The higher the hafnium concentration, the more severe the issue is. However, there is no absolute guarantee that hafnium will be the basis of future high-k dielectrics. The 2006 ITRS roadmap predicts the implementation of high-k materials to be commonplace in the industry by 2010.

1.6. **Overview of this thesis**

In this thesis several high-k materials such as, HfO₂, TiO₂, Y₂O₃, Al₂O₃ as well as composite metal oxides, HfₓYᵧO₂, HfₓTi₁₋ₓO₂, will be discussed, with the focuses on the ALD process conditions, film structure change induced by post-deposition annealing or dopants, the composition-structure-dielectric properties, etc. Chapter 2 represents background information for thin film deposition techniques; important applications of atomic layer deposition in semiconductor processing; recent innovations in high-k gate oxide research and future challenges. In chapter 3, there will be detailed introduction of experimental designs (like ALD configuration), solid-state materials characterizations. In chapter 4.1, composition-structure-dielectric properties of Yttrium doped HfO₂ will be presented, and it will expose how the composition of yttrium dopant in the film would affect the structure and dielectric properties of YDH (yttrium doped HfO₂) films; in
chapter 4.2, the surface sputtering and post-deposition annealing effects on the HfO$_2$ and TiO$_2$ films will be investigated, along with discussion of the promising dielectric properties for both film; the chapter 4.3 is an extension of chapter 4.2, which describes how the TiO$_2$ and HfO$_2$ are alloyed together to form Hf$_x$Ti$_{1-x}$O$_2$ films, with the incorporation of TiO$_2$, the crystallization temperature of HfO$_2$ could be further increased to 1000 °C, compared with 600 °C for the pure HfO$_2$. Apart from high-k material studies, another part of this thesis focuses in the area of investigation of initial depositions of HfO$_2$ and TiO$_2$ on Silicon and Copper surface (chapter 4.4 & 4.5), which could result in selective atomic layer deposition (SALD)—based on the different initial film nucleation on different surfaces, i.e., by patterning the silicon substrate with other materials such as copper, it could result in films deposition only on desired surface area. The study of SALD is with great importance with the sense of simplifying the traditional film patterning processes without the use of photomasking, a self-assembled monolayer, soft lithography or any other surface modifications—this selective deposition is purely based on the different surfaces chemistry and thusly save the routine procedures of surface modification pre-deposition or post chemical etching.

In addition to my main research areas study (chapter 4.1-4.5), I have also contributed with two summer projects, together with a REU student and a RET fellow for some innovated studies about atomic layer deposition. In chapter 4.6, low temperature deposition of HfO$_2$ was carried out on the PMMA polymer template for the potential fabrication of HfO$_2$ nanotubes; in chapter 4.7, atomic layer deposition of ultrathin Al$_2$O$_3$
was purposed as an effective buffer layer of \( \text{Hf}_x\text{Ti}_{1-x}\text{O}_2 \) to prevent the film diffusion into the silicon upon high temperature annealing.
2. LITERATURE REVIEW

2.1. **Thin film deposition techniques**

It is no understatement to say that thin film deposition techniques have, in the past three decades, fundamentally changed both condensed matter physics and everyday life. Well established thin film technologies are used to grow the integrated circuits in our computers, cell phones, and palm pilots, while novel effects in thin films continue to be discovered and explored by both solid-state physicists and optical physicists. Many of the techniques used to grow thin films are related, and many involve physics, chemistry and technology of marvelous subtlety. In this chapter session, a general introduction of thin film deposition techniques will be given, as figure 5 shown:
Figure 5. Summary of thin film deposition methods.
MBE-Molecular Beam Epitaxy; is one of several methods of depositing single crystals. It was invented in the late 1960s at Bell Telephone Laboratories by J. R. Arthur and Alfred Y. Cho [16]. Molecular beam epitaxy takes place in high vacuum or ultra high vacuum (10−8 Pa). The most important aspect of MBE is the slow deposition rate (typically less than 1000 nm per hour), which allows the films to grow epitaxially. The slow deposition rates require proportionally better vacuum to achieve the same impurity levels as other deposition techniques. In solid-source MBE, ultra-pure elements such as gallium and arsenic are heated in separate quasi-Knudsen effusion cells until they begin to slowly sublime. The gaseous elements then condense on the wafer, where they may react with each other. In the example of gallium and arsenic, single-crystal gallium arsenide is formed. The term "beam" means that evaporated atoms do not interact with each other or vacuum chamber gases until they reach the wafer, due to the long mean free paths of the atoms.

EBEAM PVD-Electron Beam Physical Vapor Deposition (also known as Electron Beam Evaporation); is another form of physical vapor deposition in which a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum. The electron beam causes atoms from the target to transform into the gaseous phase. These atoms then precipitate into solid form, coating everything in the vacuum chamber (within line of sight) with a thin layer of the anode material. More technical details will be given in chapter 3.12.
PLD-Pulsed Laser Deposition; is a common thin film deposition (specifically a physical vapor deposition, PVD) technique where a high power pulsed laser beam is focused inside a vacuum chamber to strike a target of the material that is to be deposited. This material is vaporized from the target (in a plasma plume) which deposits it as a thin film on a substrate (such as a silicon wafer facing the target). This process can occur in ultra high vacuum or in the presence of a background gas, such as oxygen which is commonly used when depositing oxides to fully oxygenate the deposited films. While the basic-setup is simple relative to many other deposition techniques, the physical phenomena of laser-target interaction and film growth are quite complex (see Process below). When the laser pulse is absorbed by the target, energy is first converted to electronic excitation and then into thermal, chemical and mechanical energy resulting in evaporation, ablation, plasma formation and even exfoliation [17]. The ejected species expand into the surrounding vacuum in the form of a plume containing many energetic species including atoms, molecules, electrons, ions, clusters, particulates and molten globules, before depositing on the typically hot substrate.

Sputtering is a process whereby atoms are ejected from a solid target material due to bombardment of the target by energetic particles. It is commonly used for thin-film deposition, etching and analytical techniques. Physical sputtering is driven by momentum exchange between the ions and atoms in the materials, due to collisions. The incident ions set off collision cascades in the target. When such cascades recoil and reach the target surface with energy above the surface binding energy, an atom can be ejected. If the target is thin on an atomic scale the collision cascade can reach the back side of the target.
and atoms can escape the surface binding energy 'in transmission'. The average number of atoms ejected from the target per incident ion is called the sputter yield and depends on the ion incident angle, the energy of the ion, the masses of the ion and target atoms, and the surface binding energy of atoms in the target. For a crystalline target the orientation of the crystal axes with respect to the target surface is relevant.

MOCVD-Metal Organic Chemical Vapor Deposition; is a chemical vapor deposition method of thin film materials, especially compound semiconductors from the surface reaction of organic compounds or metal organics and metal hydrides containing the required chemical elements. ALD-Atomic Layer Deposition; ALD is a self-limiting (the amount of film material deposited in each reaction cycle is constant), sequential surface chemistry that deposits conformal thin-films of materials onto substrates of varying compositions. ALD is similar in chemistry to chemical vapor deposition (CVD), except that the ALD reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction. Due to the characteristics of self-limiting and surface reactions, ALD film growth makes atomic scale deposition control possible. By keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as ~0.1 Å (10 pm) per monolayer. Separation of the precursors is accomplished by pulsing a purge gas (typically nitrogen or argon) after each precursor pulse to remove excess precursor from the process chamber and prevent 'parasitic' CVD deposition on the substrate. More details about ALD will be introduced in chapter 3.11.
2.2. **Applications of ALD in Semiconductor processing**

Atomic layer deposition (ALD) of ultrathin high-K dielectric films has penetrated research and development lines of several major memory and logic manufacturers due to the promise of unprecedented control of thickness, uniformity, quality and material properties. As critical layers in leading-edge devices scale to the nanometer regime, ALD is becoming recognized as not only an enabling technology, but also as the only viable technology for applications such as the gate dielectric and copper carrier/seed layers at and beyond the 32nm product generations. With the capabilities of this nanoprocessing technique having finally intersected with the technological demands of the marketplace, ALD is establishing additional inroads to the manufacturing floor, as well as other applications outside of mainstream semiconductor processing.

ALD in gate dielectric application—in the year 2007, Intel announced that their 45 nm generation processors will include a high-k HfO$_2$ gate dielectric made by ALD. There are various reasons that ALD has become the method of choice [18]. Unlike ALD, conventional evaporated films suffer from porosity and sputtering creates defects in the sensitive silicon surface layer. In addition, ALD guarantees extremely uniform and reproducible thickness, low stress, uniform stoichiometry, amorphous structure and low defect density. Besides the industrial silicon platforms, ALD has proven essential to create gate dielectrics on device substrates without native oxides, such as high mobility GaAs/AlGaAs heterostructures, organic transistors, nanotubes and many more. Examples of materials include HfO$_2$, ZrO$_2$, Al$_2$O$_3$, LaAlO, GdScO$_3$, their nanolaminates, and others.
Atomic layer deposition (ALD) will be used in multiple areas of the 22nm logic process flow despite initial concerns about the technology's viability for high-volume manufacturing. Each application space creates a unique need for manufacturing equipment configuration and technology variations – from single-wafer ALD systems for extremely tight process control, batch ALD systems for low COO operation, to mini-batch systems for a meld of COO and process control for multi-layer applications. Selection of the appropriate manufacturing toolset is as critical to eventual technology adoption as the process itself, and final implementation will require the correct toolsets to ensure that the ALD films can be deposited in a cost efficient manner.

DRAM manufacturers were the first to use ALD to ensure conformal deposition of high-k dielectrics in high aspect ratio capacitor structures. Aggressive scaling of device dimensions and the subsequent requirement of low thermal budgets to control dopant diffusion continue to push the entire semiconductor industry to displace conventional CVD, plasma enhanced CVD (PECVD), and sputtering techniques with novel ALD processes in critical areas such as transistor gate stack formation and spacer defined double patterning. The low throughputs that are typically associated with ALD techniques have been a barrier to its adoption in mainstream production flows. However, these concerns are being addressed by intelligent equipment design to optimize the ALD process and hardware for individual application spaces. At the 22nm node, the logic industry will use ALD in several key process steps – both in front end transistor formation and in back end metallization and interconnect. Each application has highly
specific requirements and calls for different hardware configurations for the optimal production solution.

Single-wafer ALD chambers are ideal when the application demands extremely thin films with precise thickness and uniformity control. Single-wafer systems can also most easily handle difficult precursor chemistries such as low vapor pressure, decomposition prone liquids and solids since ALD cycle times are typically short (in the order of a few seconds) and the source delivery systems can be placed in close proximity to the reaction chamber. Purge efficiency can be optimized relatively easily in single-wafer systems and as a result, these chambers are ideal for pure ALD deposition.
Figure 6. Need for complete ALD high-k/metal gate solution in 22 nm Logic transistors [19].
2.3. **Area Selective ALD**

While ALD inherently provides nano-scale control of materials in the vertical direction, the area-selective ALD (SALD) technique enables nano-scale definition of the lateral structure. The SALD could be achieved by controlling the substrate surface chemistry in order to impart spatial selectivity to ALD. The area selective ALD process differs from conventional photoresist-based lithography in that rather than a subtractive process; it is an additive process in which material is deposited only where needed. Because of this distinction, area selective ALD may provide a number of advantages, including reducing the number of etch and lithography steps for system utilizing multiple depositions, eliminating the need to etch difficult materials, and minimizing the use of expensive reagents.

SALD is a more efficient process in that it eliminates the selective removal steps often involving combinations of chemical etch with expensive reagents and photolithography. For this reason, there is a lot of interest in selective deposition techniques. The most common approach of SALD is to provide a molecular mask over selected non-deposited areas. In recent years several self assembled monolayer materials have been effective in preventing deposition \(^{20}\); specifically for the ALD of HfO\(_2\), several self-assembled monolayers (SAMs) have been evaluated \(^{21}\). However, SAMs typically have long assembly times of the order of hours before impervious layer is established to fully prevent deposition and require removal after deposition. An alternate and more efficient approach to SALD is to take advantage of the different materials at the surface having different nucleation times for film growth by ALD. For example, the ALD
of HfO2 on bare silicon exhibits an inhibited growth due to lack of hydroxyl surface sites for ALD; however, in this case the nucleation time is quite short and on the order of only a couple of ALD cycles \(^{22}\). Nonetheless, surprisingly this surface dependence for different materials has not been evaluated at length despite the useful benefit especially as deposited layers approach a few nanometers thickness.

2.4. **Recent renovations of High-k, Metal Gate and CMOS technologies**

2.4.1. **Gate first technology**

In the early days of the quest for a HK/MG CMOS solution, a rather disruptive approach based on the complete silicidation of the poly-silicon gate electrode, called FUSI, was proposed \(^{23}\). This approach, very promising at first due to its integration simplicity, was abandoned later on due to the difficulty in controlling the silicide phase to achieve low VT devices. Today, two main integration options remain: gate-first (often referred to as MIPS, metal inserted poly-silicon) and gate-last (also called RMG, replacement metal gate). As figure 7 shows, the terminology 'first' and 'last' refers to whether the metal electrode is deposited before or after the high temperature activation anneal(s) of the flow.

The gate-first approach was initially developed by Sematech and the IBM-led Fishkill Alliance. It relies on very thin capping layers — Al\(\text{2}O_3\) for the PMOS and LaO\(\text{x}\) for the NMOS transistors — to create dipoles that set the threshold voltage of the device. However, thermal instabilities in HK/MG devices were reported and can lead to threshold voltage shifts and re-growth in the gate stack. This issue is particularly acute for pMOS at
scaled EOT. At those aggressive EOT, it is clear that RMG can deliver significantly higher EWF (meaning lower pMOS VT) than MIPS. Note that this specific issue impedes essentially the use of gate-first for high performance applications. For low power (LSTP) or DRAM applications, where VT and EOT requirements are typically more relaxed, gate-first remains a very viable and promising option for integrating a cost effective HK/MG CMOS solution.
Figure 7. High-k first, gate-last scheme [23]
2.4.2. Gate last technology

In a gate-last process, the high-k material is deposited dummy gates are created, followed by source/drain formation and an inter level dielectric (ILD) deposition and polish. The dummy gates are removed and different work function metals are deposited for NMOS and PMOS. Companies that have reported on a gate-first process include IBM, UMC, Panasonic, Renesas, while gate-last processes have been reported by Intel and TSMC. Hoffman said a third approach, full silicidation (FUSI), where a polysilicon gate is totally converted to a silicide, has been abandoned due to a too-narrow process window. An interesting alternative described by Hoffman that achieves high Vt with scaled effective oxide thickness for PMOS is channel engineering. He said a SiGe channel process would allow gate-first process strategy, and would require only one capping layer instead of two. An on-going problem with HKMG, first reported by SEMATECH, is flat-band voltage roll-off. "As the flat-band voltage is rolling off, the PMOS Vt is going up again," Hoffman said. This problem is caused by oxygen vacancies/defects in the high-k material, which can diffuse and interlayer growth. There are two approaches to solving this problem, he noted. Since it's a thermally activated issue, going to lower or neutral thermal budgets would help. This might mean going from a spike anneal, for example, to a laser anneal. The second solution is to passivate by oxygenation, either lateral oxygenation after source/drain activation, or oxygenation through a thin layer of TiN.

2.4.3. Dual-channel CMOS for (sub)-22 nm high performance logic

The end of 2007 marked the birth of what Gordon Moore described as the “biggest change in transistor technology in 40 years,” namely the 45-nm CMOS
generation. Now in production, this technology features a transistor gate with a metal/high-k dielectric combination instead of polySi/SiO₂, which was long considered irreplaceable. If the heart of the transistor, the gate dielectric, can be changed, any other part of the transistor can be changed eventually as well. The active channel may be the next component to be replaced in an effort to surpass the performance of the 22-nm node.

Charge carriers of germanium feature higher mobility, so replacing silicon in the channel with germanium could enhance transistor performance significantly. Unfortunately, after five years of intensive research, it has now been established that Ge is suitable only for pMOS. Therefore a complementary MOS technology made entirely of Ge is not yet feasible today. Conversely, other semiconductors such as III-V compounds (e.g. GaAs, InGaAs) are indeed suitable for nMOS, but appear to be unsuitable for pMOS. Contrary to what was believed only a few years ago, semiconductors composed of Ge and III-V compounds are not competitors; rather, these materials could complement each other on the same chip.

Based on these findings, the DUALLOGIC project will attempt to cointegrate Ge pMOS and III-V nMOS side-by-side on a complexly engineered substrate on silicon to demonstrate for the first time a dual-channel CMOS technology. A European consortium of 9 members has been awarded an EC grant of 5.8 M€ for this project. All the necessary resources and expertise have been gathered for the 36-month collaboration to tackle such a challenging goal. The main objective is to demonstrate that a high-mobility, dual-channel, front-end-of-line (FEOL) CMOS technology is scalable and manufacturable. To
achieve this, researchers will employ a Si-compatible process in a 65-nm/200-mm pilot line. Researchers expect that, by the end of 2009, the DUALLOGIC project will determine whether this approach is a viable option for CMOS beyond 22 nm. The results could stimulate further development into a wider sub-22-nm technology platform by integrating dual-channel FEOL with backend and device-architecture modules. Such results could provide a solid basis for a future, even more comprehensive R&D initiative in Europe. DUALLOGIC, a top ranked project, is the "flagship of CMOS in FP7 (the European Commission’s 7th Framework Program). The aim is to develop a high mobility dual-channel Front-End of Line technology as an option for (sub)-22 nm high performance logic ICs. Unlike the present day devices which are all made of Si, I have propose that the active channel of pMOS and nMOS transistors in future nanoelectronics could be made of different high mobility semiconductor materials. In particular, they proposed that pMOS are made of Ge and nMOS are made of III-V compound semiconductors co-integrated in the same complex engineered substrate as shown in the Figure below.
Figure 8. The structure of the proposed Dual-channel CMOS logic \cite{24}.
3. EXPERIMENTATION AND CHARACTERIZATION TECHNIQUES

3.1. Applied thin film deposition techniques

3.1.1. Custom made & constructed ALD system

The ALD was performed in a hot wall tubular reactor as figure 9 shown. The reactor consists of a high purity quartz tube (38 mm diameter x 480 mm long) with a quartz tube (could withstand temperature over 1000 °C) serving as a substrate holder. The manifold has two separate lines for moisture and precursor leading into the reactor. During a single ALD cyclic reaction, a tiny amount of precursor vapor and moisture will be alternatively pulsed into reaction chamber with through N₂ gas purge in between to make sure of the formation of only one monolayer after each cyclic reaction. The reactant moisture was provided by DI water (>18 MΩ·cm) kept in ice bath, which used to guarantee the same amount of moisture in each pulse. In this ALD system, N₂ not only serves as precursors (metal precursors and moisture) but also used to vent the gate for loading & unloading samples—the valve designed specifically for gate venting is closed during deposition.

The present system was upgraded from the old system with only two precursor canisters by adding the third precursor canister with sharing the same pneumatic valve with precursor B. While such design saved the cost of an expensive pneumatic valve, but it confines the application for depositing ternary metal oxide composition films. It may serves as depositing a buffer layer of metal (C) oxide and then deposition binary metal (AB) oxide on C, or depositions of binary oxide AB, BC and AC. The operating pressure
of this deposition system ranges from 0.2 to 1.5 torr and the base pressure is about 0.01 torr.

A single ALD cyclic reaction consists of four steps: (i) exposure of the first precursor (usually the metal precursor); (ii) purge the reactor with N₂; (iii) exposure of the second precursor (moisture in such case); (v) purge reactor. In the first step, the precursor molecule in the gas phase will chemisorbed on the substrate forming a over saturated monolayer of precursor molecules, in the following step, the reactor will be evacuated resulting the monolayer formation of precursor molecule on the substrate, in step three, the second precursor will be pulsed into reactor and it will undergo interchange reaction with the first reactant and forms metal oxide layer as well as side products, in step four, the reaction chamber will be purged again leaving only one monolayer of metal oxide. Repeating cycle will be performed until reach the wanted film thickness. The reaction cycle number, pulse time for each precursor and purging time are controlled by labview program, and the user will be responsible for optimizing those parameters and input different numbers as desired.
Figure 9. Scheme of the custom designed & made ALD reactor with capacity for depositing two different metal oxides (HfO₂/Y₂O₃, HfO₂/TiO₂).

**Operating Pressure = 0.2-1.5 Torr**

**Moisture pulse = 0.05 s**
3.1.2. **Electron Beam Evaporation System**

Electron Beam Evaporation is a form of physical vapor deposition in which a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum. The electron beam causes atoms from the target to transform into the gaseous phase. These atoms then precipitate into solid form, coating everything in the vacuum chamber (within line of sight) with a thin layer of the anode material.

Thin film deposition is a process applied in the semiconductor industry to grow electronic materials, in the aerospace industry to form thermal and chemical barrier coatings to protect surfaces against corrosive environments, in optics to impart the desired reflective and transmissive properties to a substrate and elsewhere in industry to modify surfaces to have a variety desired properties. The PVD process can be carried out at lower deposition temperatures and without corrosive products, but deposition rates are typically lower. Electron beam physical vapor deposition, however, yields a high deposition rate from 0.1 μm / min to 100 μm / min $[^{25}]$ at relatively low substrate temperatures, with very high material utilization efficiency. The schematic of an EBPVD system is shown in Fig 10.
Figure 10. Scheme of Electron Beam Evaporation. (figure downloadable at http://en.wikipedia.org/wiki/Electron_beam_physical_vapor_deposition)
Evaporation involves two basic processes: a hot source material evaporates and condenses on the substrate. It resembles the familiar process by which liquid water appears on the lid of a boiling pot. However, the gaseous environment and heat source (see "Equipment" below) are different. Evaporation takes place in a vacuum, i.e. vapors other than the source material are almost entirely removed before the process begins. In high vacuum (with a long mean free path), evaporated particles can travel directly to the deposition target without colliding with the background gas. (By contrast, in the boiling pot example, the water vapor pushes the air out of the pot before it can reach the lid.) At a typical pressure of 10-4 Pa (10-7 Pa in this case), an 0.4-nm particle has a mean free path of 60 m. Hot objects in the evaporation chamber, such as heating filaments, produce unwanted vapors that limit the quality of the vacuum.

3.1.3. **Three-zone post deposition annealing furnace**

Post deposition annealing and forming gas (%5 H\textsubscript{2} and 95 % N\textsubscript{2} as balance gas) annealing were performed in a three-zone Lindberg Blue horizontal hot-walled furnace (with Maximum temperature annealing to 1100 °C). At the inlet of the furnace, a removal cap is equipped for loading and unloading samples in a quartz tube, which could stand high temperature annealing above 1000 °C. The Lindberg/Blue has three equally long annealing zones of 24” in the middle of the furnace with each zone’s temperature controlled independently. The post deposition annealing was under the ambient condition of N\textsubscript{2} (99.996%) with constant flow rate at about 44 sccm. Prior to annealing, the chamber of the furnace is purged with N\textsubscript{2} for 15 min after reaching the set temperature and then sample was loaded into the center of the furnace tube. The typical annealing
time was set for 5 min, which is good enough for altering the crystal structure of certain metal oxide films at certain annealing temperatures. In the case of forming gas annealing, the recipe is similar—after purging the furnace chamber for 15 min with N₂, the gas flow will be switched to H₂/N₂. For safety issues, the exhaust of forming gas was directed led to the fume rather than discharging into the air.
Figure 11. Scheme of three zone furnace used for post deposition and forming gas.
3.2. **Characterization techniques**

3.2.1. **Spectral Ellipsometry (SE)**

Ellipsometry is primarily interested in how p- and s- components change upon reflection or transmission in relation to each other. In this manner, the reference beam is part of the experiment. A known polarization is reflected or transmitted from the sample and the output polarization is measured. The change in polarization is the ellipsometry measurement, commonly written as \[26\]:

\[
\rho = \tan(\psi) e^{i\Delta}
\]  

(3.1)

A sample ellipsometry measurement is shown in Figure 12. The incident light is linear with both p- and s- components. The reflected light has undergone amplitude and phase changes for both p- and s- polarized light, and ellipsometry measures their changes.

The primary tools for collecting ellipsometry data all include the following: light source, polarization generator, sample, polarization analyzer, and detector. The polarization generator and analyzer are constructed of optical components that manipulate the polarization: polarizers, compensators, and phase modulators. Common ellipsometer configurations include rotating analyzer (RAE), rotating polarizer (RPE), rotating compensator (RCE), and phase modulation (PME).
Figure 12. Typical ellipsometry configuration, where linearly polarized lights reflected from the sample surface and the polarization change is measured to determine the sample response
The RAE configuration is shown in Figure 13. A light source produces unpolarized light which is then sent through a polarizer. The polarizer allows light of a preferred electric field orientation to pass. The polarizer axis is oriented between the p- and s- planes, such that both arrive at the sample surface. The linearly polarized light reflects from the sample surface, becomes elliptically polarized, and travels through a continuously rotating polarizer (referred to as the analyzer). The amount of light allowed to pass will depend on the polarizer orientation relative to the electric field “ellipse” coming from the sample. The detector converts light to electronic signal to determine the reflected polarization. This information is compared to the known input polarization to determine the polarization change caused by the sample reflection. This is the ellipsometry measurement of Psi and Delta.
Figure 13. Rotating analyzer ellipsometer configuration uses a polarizer to define the incoming polarization and a rotating polarizer after the sample to analyze the outgoing light. The detector converts light to a voltage whose dependence yields the measurement of the reflected polarization.
Ellipsometry measures changes in light polarization to determine the sample material's properties of interest, such as film thickness and optical constants. In the case of a bulk material, the equations derived for a single reflection can be directly inverted to provide the “pseudo” optical constants from the ellipsometry measurement [27]:

\[
\langle \varepsilon \rangle = \sin^2(\phi) \left[ 1 + \tan^2(\phi) \left( \frac{1 - \rho}{1 + \rho} \right) \right]
\]  

(3.2)

This equation assumes there are no surface layers of any type. However, in any bulk material, there is typically a surface oxide or roughness, and the direct inversion would include these as part of the bulk optical constants. The more common procedure used to deduce material properties from ellipsometry measurements following the flow chart in Figure 14. Regression analysis is required because an exact equation cannot be written. Often the answer is over-determined with hundreds of experimental data points for a few unknowns. Regression analysis allows all of the measured data to be included when determining the solution.
Figure 14. Flowchart for ellipsometry data analysis (figure 12, 13 & 14)

Downloadable at http://www.jawoollam.com/
Data analysis proceeds as follows: After a sample is measured, a model is constructed to describe the sample. The model is used to calculate the predicted response from Fresnel’s equations which describe each material with thickness and optical constants. If these values are not known, an estimate is given for the purpose of the preliminary calculation. The calculated values are compared to experimental data. Any unknown material properties can then be varied to improve the match between experiment and calculation. The number of unknown properties should not exceed the amount of information contained in the experimental data. For example, a single-wavelength ellipsometer produces two data points (Ψ, Δ) which allows a maximum of two material properties to be determined. Finding the best match between the model and the experiment is typically achieved through regression. An estimator, like the Mean Squared Error (MSE), is used to quantify the difference between curves. The unknown parameters are allowed to vary until the minimum MSE is reached.

3.2.2. **X-ray Photoelectron Spectroscopy (XPS)**

X-ray photoelectron spectroscopy (XPS) is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the material being analyzed. XPS requires ultra high vacuum (UHV) conditions.
XPS is a surface chemical analysis technique that can be used to analyze the surface chemistry of a material in its "as received" state, or after some treatment, for example: fracturing, cutting or scraping in air or UHV to expose the bulk chemistry, ion beam etching to clean off some of the surface contamination, exposure to heat to study the changes due to heating, exposure to reactive gases or solutions, exposure to ion beam implant, exposure to ultraviolet light.
Figure 15. Basic component of a monochromatic XPS system
Monochromatic system (as figure 15 shown) with aluminum K-alpha X-rays are normally produced by diffracting and focusing a beam of non-monochromatic X-rays off of a thin disc of natural, crystalline quartz with a <1010> orientation. The resulting wavelength is 8.3386 angstroms (0.83386 nm) which corresponds to a photon energy of 1486.7 eV. The energy width of the monochromatic X-rays is 0.16 eV, but the common electron energy analyzer (spectrometer) produces an ultimate energy resolution on the order of 0.25 eV which, in effect, is the ultimate energy resolution of most commercial systems. When working under practical, everyday conditions, high energy resolution settings will produce peak widths (FWHM) between 0.4–0.6 eV for various pure elements and some compounds.

Non-monochromatic magnesium X-rays have a wavelength of 9.89 angstroms (0.989 nm) which corresponds to a photon energy of 1253 eV. The energy width of the non-monochromated X-ray is roughly 0.70 eV, which, in effect is the ultimate energy resolution of a system using non-monochromatic X-rays. Non-monochromatic X-ray sources do not use any crystals to diffract the X-rays which allows all primary X-rays lines and the full range of high energy Bremsstrahlung X-rays (1–12 keV) to reach the surface. The typical ultimate high energy resolution (FWHM) when using this source is 0.9–1.0 eV, which includes with the spectrometer-induced broadening, pass-energy settings and the peak-width of the non-monochromatic magnesium X-ray source.

3.2.3. **Grazing Incidence X-ray Diffraction**

X-ray diffraction yields the atomic structure of materials and is based on the elastic scattering of X-rays from the electron clouds of the individual atoms in the system.
The most comprehensive description of scattering from crystals is given by the dynamical theory of diffraction \(^28\).

Single-crystal X-ray diffraction is a technique used to solve the complete structure of crystalline materials, ranging from simple inorganic solids to complex macromolecules, such as proteins. Powder diffraction (XRD) is a technique used to characterize the crystallographic structure, crystallite size (grain size), and preferred orientation in polycrystalline or powdered solid samples. Powder diffraction is commonly used to identify unknown substances, by comparing diffraction data against a database maintained by the International Centre for Diffraction Data. It may also be used to characterize heterogeneous solid mixtures to determine relative abundance of crystalline compounds and, when coupled with lattice refinement techniques, such as riveted refinement, can provide structural information on unknown materials. Powder diffraction is also a common method for determining strains in crystalline materials. An effect of the finite crystallite sizes is seen as a broadening of the peaks in an X-ray diffraction as is explained by the Scherrer Equation.

Thin film diffraction and grazing incidence X-ray diffraction may be used to characterize the crystallographic structure and preferred orientation of substrate-anchored thin films. High-resolution X-ray diffraction is used to characterize thickness, crystallographic structure, and strain in thin epitaxial films. It employs parallel-beam optics. X-ray pole figure analysis enables one to analyze and determine the distribution of
crystalline orientations within a crystalline thin-film sample. X-ray rocking curve analysis is used to quantify grain size and mosaic spread in crystalline materials.

3.2.4. Fourier Transformed Infra Red (FTIR)

Fourier transform infrared (FTIR) spectroscopy \cite{29} is a technique which is used to obtain an infrared spectrum of absorption, emission, photoconductivity or Raman scattering of a solid, liquid or gas. An FTIR spectrometer simultaneously collects spectral data in a wide spectral range. This confers a significant advantage over a dispersive spectrometer which measures intensity over a narrow range of wavelengths at a time. FTIR technique has made dispersive infrared spectrometers all but obsolete (except sometimes in the near infrared) and opened up new applications of infrared spectroscopy.

The term Fourier transform infrared spectroscopy originates from the fact that a Fourier transform (a mathematical algorithm) is required to convert the raw data into the actual spectrum. For other uses of this kind of technique, see Fourier transform spectroscopy.
Figure 16. (a) Phillips X-pert XRD instrument at CMM, Urbana

(b) GIXRD arrangement illustration of experimental configuration.

(figures downloadable at http://cmm.mrl.uiuc.edu/)
In this work, Fourier Transform Infrared Spectroscopy (Nicolet, Magna-IR 560) was used in the normal transmission mode over the wave-number range of 4000 to 400 cm\(^{-1}\). Spectra of cleaned wafer prior to deposition were used for background subtraction from spectra of post deposition and annealed samples. After spectral subtraction, the FTIR spectra reveal information about the deposited film and changes after all kinds of post treatment like annealing.
Figure 17. The picture of FTIR Nicolet, Magna-IR 560 system
3.2.5. Scanning Electron Microscopy (SEM)

The scanning electron microscope (SEM) is a type of electron microscope that images the sample surface by scanning it with a high-energy beam of electrons in a raster scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition and other properties such as electrical conductivity.

The types of signals produced by an SEM include secondary electrons, back-scattered electrons (BSE), characteristic X-rays, light (cathodoluminescence), specimen current and transmitted electrons. Secondary electron detectors are common in all SEMs, but it is rare that a single machine would have detectors for all possible signals. The signals result from interactions of the electron beam with atoms at or near the surface of the sample. In the most common or standard detection mode, secondary electron imaging or SEI, the SEM can produce very high-resolution images of a sample surface, revealing details about less than 1 to 5 nm in size. Due to the very narrow electron beam, SEM micrographs have a large depth of field yielding a characteristic three-dimensional appearance useful for understanding the surface structure of a sample. This is exemplified by the micrograph of pollen shown to the right. A wide range of magnifications is possible, from about 10 times (about equivalent to that of a powerful hand-lens) to more than 500,000 times, about 250 times the magnification limit of the best light microscopes. Back-scattered electrons (BSE) are beam electrons that are reflected from the sample by elastic scattering. BSE are often used in analytical SEM along with the spectra made from the characteristic X-rays. Because the intensity of the BSE signal is strongly related
to the atomic number (Z) of the specimen, BSE images can provide information about the
distribution of different elements in the sample. For the same reason, BSE imaging can
image colloidal gold immuno-labels of 5 or 10 nm diameter which would otherwise be
difficult or impossible to detect in secondary electron images in biological specimens.
Characteristic X-rays are emitted when the electron beam removes an inner shell electron
from the sample, causing a higher energy electron to fill the shell and release energy.
These characteristic X-rays are used to identify the composition and measure the
abundance of elements in the sample.

All samples must also be of an appropriate size to fit in the specimen chamber and
are generally mounted rigidly on a specimen holder called a specimen stub. Several
models of SEM can examine any part of a 6-inch (15 cm) semiconductor wafer, and some
can tilt an object of that size to 45°. For conventional imaging in the SEM, specimens
must be electrically conductive, at least at the surface, and electrically grounded to
prevent the accumulation of electrostatic charge at the surface. Metal objects require little
special preparation for SEM except for cleaning and mounting on a specimen stub.
Nonconductive specimens tend to charge when scanned by the electron beam, and
especially in secondary electron imaging mode, this causes scanning faults and other
image artifacts. They are therefore usually coated with an ultrathin coating of electrically-
conducting material, commonly gold, deposited on the sample either by low vacuum
sputter coating or by high vacuum evaporation. Conductive materials in current use for
specimen coating include gold, gold/palladium alloy, platinum, osmium,[30] iridium,
tungsten, chromium and graphite. Coating prevents the accumulation of static electric charge on the specimen during electron irradiation.

Two reasons for coating, even when there is enough specimen conductivity to prevent charging, are to increase signal and surface resolution, especially with samples of low atomic number (Z). The improvement in resolution arises because backscattering and secondary electron emission near the surface are enhanced and thus an image of the surface is formed.
Figure 18. The picture of Hitachi S-3000N system (UIC RRC-WEST)
3.2.6. Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique whereby a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through. An image is formed from the interaction of the electrons transmitted through the specimen; the image is magnified and focused onto an imaging device, such as a fluorescent screen, on a layer of photographic film, or to be detected by a sensor such as a CCD camera.

TEMs are capable of imaging at a significantly higher resolution than light microscopes, owing to the small de Broglie wavelength of electrons. This enables the instrument's user to examine fine detail—even as small as a single column of atoms, which is tens of thousands times smaller than the smallest resolvable object in a light microscope. TEM forms a major analysis method in a range of scientific fields, in both physical and biological sciences. TEMs find application in cancer research, virology, materials science as well as pollution and semiconductor research.

At smaller magnifications TEM image contrast is due to absorption of electrons in the material, due to the thickness and composition of the material. At higher magnifications complex wave interactions modulate the intensity of the image, requiring expert analysis of observed images. Alternate modes of use allow for the TEM to observe modulations in chemical identity, crystal orientation, electronic structure and sample induced electron phase shift as well as the regular absorption based imaging.
Figure 19. (a) Picture of TEM JEOL 3010F (UIC RRC-EAST). (b) Scheme of TEM configuration (pictures downloadable at http://www.rrc.uic.edu/)
Theoretically, the maximum resolution, $d$, that one can obtain with a light microscope has been limited by the wavelength of the photons that are being used to probe the sample, $\lambda$, and the numerical aperture of the system, NA.$^{[31]}$

$$d = \frac{\lambda}{2\pi \sin \alpha} \approx \frac{\lambda}{2NA}$$ (3.3)

Early twentieth century scientists theorized ways of getting around the limitations of the relatively large wavelength of visible light (wavelengths of 400–700 nanometers) by using electrons. Like all matter, electrons have both wave and particle properties (as theorized by Louis-Victor de Broglie), and their wave-like properties mean that a beam of electrons can be made to behave like a beam of electromagnetic radiation. The wavelength of electrons is found by equating the de Broglie equation to the kinetic energy of an electron. An additional correction must be made to account for relativistic effects, as in a TEM an electron's velocity approaches to the speed of light, $c$.\[^{[32]}\]

$$\lambda_e \approx \frac{h}{\sqrt{2m_0E\left(1 + \frac{E}{2m_0c^2}\right)}}$$ (3.4)

Where, $h$ is Planck’s constant, $m_0$ is the rest mass of an electron and $E$ is the energy of the accelerated electron. Electrons are usually generated in an electron microscope by a process known as thermionic emission from a filament, usually tungsten, in the same manner as a light bulb, or alternatively by field electron emission.$^{[33]}$ The electrons are then accelerated by an electric potential (measured in volts) and focused by
electrostatic and electromagnetic lenses onto the sample. The transmitted beam contains information about electron density, phase and periodicity; this beam is used to form an image.

3.2.7. **Optical Profilometry-Phase Shift Interferometry (PSI)**

Interferometry refers to a family of techniques in which electromagnetic waves are superimposed in order to extract information about the waves. An instrument used to interfere waves is called an interferometer. Interferometry is an important investigative technique in the fields of astronomy, fiber optics, engineering metrology, optical metrology, oceanography, seismology, quantum mechanics, nuclear and particle physics, plasma physics, remote sensing and biomolecular interactions.\[^{34}\] Interferometry makes use of the principle of superposition to combine separate waves together in a way that will cause the result of their combination to have some meaningful property that is diagnostic of the original state of the waves. This works because when two waves with the same frequency combine, the resulting pattern is determined by the phase difference between the two waves—waves that are in phase will undergo constructive interference while waves that are out of phase will undergo destructive interference. Most interferometers use light or some other form of electromagnetic wave.\[^{35}\]

An idealized interferometric determination of wavelength obtained by looking at interference fringes between two coherent beams recombined after traveling different distances. (The square red emitter is a laser.) Typically a single incoming beam of coherent light will be split into two identical beams by a grating or a partial mirror. Each
of these beams will travel a different route, called a path, until they are recombined before arriving at a detector. The path difference, the difference in the distance traveled by each beam, creates a phase difference between them. It is this introduced phase difference that creates the interference pattern between the initially identical waves. If a single beam has been split along two paths then the phase difference is diagnostic of anything that changes the phase along the paths. This could be a physical change in the path length itself or a change in the refractive index along the path.
Figure 20. Scheme of light path through an interferometer
Wyko surface profiler (Wyko NT 3000) system is non-contact optical profiler that uses two technologies to measure a wide range of surface height. Phase-shift interferometry (PSI) mode allows you to measure smooth surfaces and small steps, while vertical scanning interferometry (VSI) mode allows you to measure rough surfaces and steps up to several millimeters high.

Phase-shifting interferometry (PSI) is not a new technique. In phase-shifting interferometry, a white light beam is filtered and passed through an interferometer objective to the test surface. The interferometer beam splitter reflects half of the incident beam to the reference surface within the interferometer. The beams reflected from the rest surface and the reference surface recombine to form interference fringes. These fringes are the alternating light and dark bands you see when the surface is in focus (as figure 20 shown).
4. RESULTS AND DISCUSSION

4.1. Composition-structural-dielectric Properties of Atomic Layer Deposited Yttrium Doped Hafnium Oxide Films

4.1.1. Introduction

The study of ultrathin structures of new high-dielectric constant materials is the key to success in the future fabrication of semiconductor devices such as in complementary metal oxide semiconductors (CMOS) and dynamic random access memory (DRAM). The use of traditional silicon dioxide as a gate dielectric insulating layer has reached its fundamental limits in terms of gate-controlled mobility without excess leakage current or gate channel diffusion [36, 37]. These problems need to be solved by finding alternative materials with high-dielectric constant (κ), negligible leakage current, and good chemical compatibility with silicon. In the last few years, hafnium oxide (κ~20) has been used as the new high dielectric constant material for the gate dielectric layer in the future transistors and capacitive memory cells. However, further device scaling necessary for maintaining Moore’s law [38] requires dielectric materials with even higher permittivity while maintaining negligible leakage current and good stability with silicon. Interestingly, the cubic and tetragonal crystalline structures of hafnium oxide hold promise because of their higher permittivity based on theoretical calculations [39]. Typically, these structures are attainable in pure HfO₂ only at very high temperatures (T>1750 °C and T>2700 °C, respectively) [40]. However, recent studies have shown that the incorporation of other metal oxides [41], such as yttrium oxide [42-44] into HfO₂ films can allow a pathway to obtain these high permittivity structures at much lower temperatures amenable to semiconductor manufacturing. This could extend...
capabilities of HfO$_2$-based films as longer term solutions for addressing the need for higher dielectric films in semiconductor devices.

A detailed composition-structure-dielectric property investigation needs to be done for the promising yttrium doped HfO$_2$ (YDH) thin films in order to understand dependence of yttrium content on post annealed structures and resulting dielectric properties. Such a study requires a deposition process that is robust and provides strong control of the composition. Compared to pulsed laser deposition [$^{45}$], electron beam evaporation [$^{46}$] and chemical vapor deposition [$^{47}$], sub-monolayer control of the deposition process makes atomic layer deposition (ALD) an ideal technique for this study and future optimization of yttrium-doped HfO$_2$ films. The incorporation of Y$_2$O$_3$ in HfO$_2$ has been previously studied using different deposition techniques and yttrium doping in HfO$_2$ has been observed to increase the dielectric constant to different degrees. For instance, Dai et al [$^{48}$] used pulsed laser deposition to deposit epitaxial yttrium-stabilized hafnia films on a silicon substrate at 550 °C and observed a permittivity of 14; however, in this case, the amount of yttrium in the film was not reported. Rauwel et al [$^{42}$] used chemical vapor deposition to grow YDH films with various Y percentages (2.0 ~ 99 at %) and substrate temperatures (470-600 °C). They observed the resulting films to have a cubic HfO$_2$ structure when yttrium content is greater than 2.5 atomic % at substrate temperature of 600 °C; however, a mixed monoclinic/cubic phase was reported at this substrate temperature with the yttrium content of 2.5 %. Furthermore, they observed a maximum $\kappa$ value of $\sim$22 at a 6.5-10 atom % of yttrium in HfO$_2$ and conjectured the presence of silicate, which may be responsible for reducing the permittivity of the film.
Kita et al. \cite{43} co-sputtered HfO$_2$ and Y$_2$O$_3$ to deposit YDH films with 0, 4, and 17% yttrium in HfO$_2$ and observed the 4 atom % yttrium in HfO$_2$ to have the largest permittivity ($\kappa \sim 27$). Yang et al. \cite{44} used molecular beam epitaxy to grow single crystal YDH films with cubic structure on GaAs(001) substrate without annealing despite the lattice mismatch of ~9.4%. The single crystal YDH film in their study had an atomically sharp interface with GaAs substrate and exhibited a maximum dielectric constant of 32 at a 19% yttrium dopant level with a leakage current of $6 \times 10^{-5}$ A/cm$^2$ at a 1 V bias voltage. Very recently, Niinisto et al. \cite{18} reported atomic layer deposition of yttrium-doped HfO$_2$ films using either (CpMe)$_2$Hf(OMe)Me or Hf(NEtMe)$_4$ with (CpMe)$_3$Y to deposit YDH films on TiN or native oxide covered silicon substrates using ozone as the oxidizer. In the limited compositional range studied in their experiments (~4-8% yttrium in the case of Hf(NEtMe)$_4$, a maximum dielectric constant of ~ 30 was achieved when measured on films deposited on TiN substrate surface using ALD cycle ratio of 20:1. From their X-ray diffraction data, only the most intense (111) reflection peak was evident leading to uncertainty in the discrimination of cubic and tetragonal phases after annealing at 500 °C, 600 °C, and 700 °C. No other structure information was reported in this study. However, dielectric constant values for YDH films on silicon substrate with native oxide or oxide-free silicon substrate were not reported in this ALD study even though such structures would be more relevant for high-κ gate oxide in CMOS technology in the semiconductor industry. A critical issue in silicon based surfaces is the presence and growth of an interfacial oxide which would undesirably lead to reduction in the overall permittivity of the structure.
In this thesis, it is reported that use of ALD to deposit YDH films with recently identified yttrium precursor, tris(ethylcyclopentadienyl) yttrium, and tetrakis(diethylamino) hafnium with water vapor as the oxidizer. I investigated the dielectric property of thin films over a wide range of compositionally tuned yttrium in HfO₂ (from 2.5% to 100% yttrium content) as function of annealing temperature (600 – 925 ºC) and performed high resolution x-ray diffraction and cross sectional transmission electron microscopy to thoroughly assess compositional, structural, and electrical properties of YDH films.

4.1.2. Experimentation

YDH thin films of various compositions were deposited using tetrakis(diethylamino) hafnium and tris(ethylcyclopentadienyl) yttrium with water vapor as the oxidizer in a hot wall tubular ALD reactor. The details of the reactor set-up have been reported elsewhere [49]. The YDH films were deposited at the reaction temperature of 250 ºC. At this temperature the individual growth rates of Y₂O₃ and HfO₂ films were 1.7 Å/cycle and 1.5 Å/cycle, respectively. The YDH films with different yttrium content were deposited by alternating one ALD cycle of Y₂O₃ deposition with a variable number of ALD cycles of HfO₂ deposition. Prior to deposition, silicon (100) substrates were cut into small squares (20mm by 20mm) and then cleaned by first soaking in 1:1:5 NH₄OH:H₂O₂: H₂O solution for 15 min to remove organic contaminants, followed by a 10 s dip in 1% HF dip, which left a ~1 nm thick native oxide layer [50]. Each of the two steps was followed by thorough DI water rinse and final drying in N₂. Immediately after the cleaning process, the substrates were placed into the ALD reactor to deposit HfO₂-
Y₂O₃ films in sequences of ALD cycles between HfO₂ and Y₂O₃. The ALD of both metal oxide films performed under same conditions have been previously reported elsewhere [49]. In the sequential ALD process used here, a number of HfO₂ ALD cycles were completed followed by another number of ALD cycles of Y₂O₃, where an ALD cycle refers to pulsed addition of precursor followed by pulsed addition of oxidizer with inert gas purged in between. The relative ratio of ALD cycles of Y₂O₃ to total ALD cycles (HfO₂ and Y₂O₃) is referred to as ALD cycle ratio. This cycle ratio has been shown to correspond approximately to the actual atom ratio of Y/Hf in a previous study [49]. In this study, the ALD cycle ratios varied from 2.5% to 100% and unless specified otherwise, relative amounts of yttrium will be expressed as ALD duty cycle. After deposition, the thickness of as-deposited films was measured using a spectral ellipsometer (J. A. Woollam Co., Inc., Model M-44). The composite films were annealed in a rapid thermal processing (RTP) furnace (Modular Process Technology, RTP-600S) at different temperatures for 5 minutes. A high-resolution X-ray diffractometer (Philips X’pert) configured with 0.15418 nm X-ray emission line of Cu with a bandwidth of 0.05 nm as the excitation source was used to obtain grazing-incidence X-ray diffraction (GIXRD) diffractogram of ~30 nm thick YDH nano-laminate films. GIXRD diffractograms were collected at a low angle of 0.7° to enhance diffraction sensitivity within the film and to avoid interference from diffraction peaks of the substrate. Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements were performed at different frequencies using Agilent 4980 equipped with mercury probe station (Materials Development Corporation, Model 802B). The capacitors formed with the mercury probe had an area of 0.46 mm². Before C-V and I-V measurements, the films were annealed in the RTP furnace at 400 °C.
for 30 min in a 5% H₂-95% N₂ atmosphere to enhance electrical performance. The interfacial structure of the YDH layer was probed using the JEOL3010 transmission electron microscope (TEM) equipped with a LaB₆ electron gun operated at 300kV.

4.1.3. Results and discussions

Grazing-incidence x-ray diffraction

The structural differences between YDH films, pure HfO₂ and pure Y₂O₃ films can be clearly observed in the GIXRD diffractograms shown in Figure 21. All YDH films prepared were around 25 nm thick and were annealed at 600 °C or 800 °C before being examined by GIXRD. Pure HfO₂, corresponding to zero cycle ratio in the sequential ALD process, crystallizes into monoclinic phase after annealing at 600 °C or 800 °C (shown by (a) in Figure 1a). When the ALD cycle ratio increases from 0 to 2.5% (by alternating 39 cycles of HfO₂ with 1 cycle of Y₂O₃), diffraction peaks at 2θ=30.6°, 35.8°, 51.1°, and 60.5° appear which correspond well to cubic-HfO₂ structure. Surprisingly, as little as 2.5% is sufficient to alter the annealed structure entirely from monoclinic to cubic phase. In the X-ray structural analysis of co-sputtered metal oxide films, Kita et al also observed a cubic phase when annealed at 600 °C for < 10 atom % Y in HfO₂ but found cubic/monoclinic mixed phase when annealed at higher temperature (1000 °C) [43]. In our studies, the sequential ALD process produced a compositionally laminated film with amorphous film structure. After annealing, the film crystallized into a polycrystalline cubic structure. As the yttrium content was further increased (up to 20%) by increasing the Y₂O₃ ALD cycle ratio, the intensities of these cubic-HfO₂ diffraction peaks increase, which indicates increased crystallinity. Upon closer examination of the diffraction line
widths of GIXRD data shown in Figure 1, they are roughly 0.5° in 2θ. Based on the Scherrer’s Equation [51],

\[
\text{Grain size (nm)} = \frac{0.9\lambda}{B\cos\theta}
\]

where \( \lambda \) is the X-ray wavelength in nm and \( B \) is the full width at half maximum in radians in terms of 2θ after correcting for instrument line width of ~0.1°, the average grain size is ~ 16 nm. This calculation assumes influence of lattice strain is negligible to grain size and any further contributions of line width due to strain would lead to larger grain sizes on average. In Figure 22, YDH film sample with 20% yttrium content subjected to different annealing temperatures (600, 800 and 925 ℃) has been examined. It is evident from the graph that all the peaks follow the same trend after each post-annealing temperature. Therefore, the cubic HfO₂ phase transformation is independent of the post-annealing temperature from 600 - 925 ℃ at this concentration of yttrium.
Figure 21. GIXRD diffractogram of ~25 nm-thick YDH films and pure hafnia and yttria films at 600 °C (21a) and 800 °C (21b) in N₂ for 5 min. The cycle ratio of laminated films varied as (a) ~ 0 (only HfO₂), (b) ~ 0.025, (c) ~ 0.05, (d) ~ 0.1, (e) ~ 0.14, (f) ~ 0.2, c: cubic; m: monoclinic
Figure 22. GIXRD diffractogram of yttria-doped HfO$_2$ film (with the cycle ratio of 0.2) annealed at different temperatures, (a) $\sim$ 600 °C, (b) $\sim$ 800 °C, (c) $\sim$ 925 °C. The thickness of the films is same as in the case of Figure 21.
**Cross-sectional TEM**

Figure 23 (a) shows a low magnification TEM image of the as-deposited film structure for the 20% YDH film. Three distinct layers can be observed. The leftmost layer is the crystalline silicon substrate. On the rightmost side, a white area is attributed to the amorphous epoxy layer. The darker layer in the center is the thin as-deposited film which is amorphous and 30 nm thick. In the region enclosed in the rectangle (see Figure 23(a)), distinct layers can be observed and indicate the compositional laminating from the ALD process. Thus after the alternating ALD deposition process, the deposited Y$_2$O$_3$ and HfO$_2$ layers remain intact and no inter-diffusion occurs under deposition temperature of 250 °C.

Figure 23 (b) and 3(c) are the high-resolution TEM images for the films annealed at 600 °C in N$_2$ atmosphere. The large bright regions (the lower left part in fig 23 (b) and the top part in fig 23 (c)) are the crystalline silicon substrates as evident from the ordered atomic arrangements. The thin layer next to the crystalline silicon is most likely silicon oxide layer$^{48}$ having a uniform thickness of ~1.5 (in fig 23 (b)) and 2.5 (in fig 23 (c)) nm. The uniform darker region is identified as the comprised of a crystalline matrix of Y$_2$O$_3$ and HfO$_2$. It is interesting to note that this region was amorphous in the case of as-deposited film with a laminate-like structure. However, after annealing this layer has crystallized and the original laminate-like structure has transformed into a more homogeneous layer. The annealed YDH structure is more akin to the formation of a hafnium oxide film with uniformly doped yttrium. It is evident that the thermal energy provided during the annealing process has caused atomic inter-diffusion resulting in the
observed homogeneity. The TEM images also show atomic fringing is prevalent in this region, which indicates crystallinity in the film, and based on the pattern of these fringes, the film appears to be polycrystalline. These TEM observations are consistent with that observed in GIXRD data.
Figure 23. (a) Low magnification (120k ×) cross-sectional TEM image of 30 nm 20% yttria doped as-deposited film. High magnification (600k ×) cross-sectional TEM image of (b) 20% yttria-doped HfO₂ film and (c) 2.5% yttria-doped HfO₂ film annealed at 600 °C for 5 min. The silicon dioxide layer at the interface has a uniform thickness (~1.5 in (b) and ~2.5 nm in (c)).
**C-V measurements**

C-V measurements were performed over a voltage range of -3 to +3 V under frequencies ranging from 5 kHz to 10 kHz. Relative permittivity ($\kappa$) values were computed from the maximum capacitance observed in the accumulation region. Figure 24 (a) shows the C-V curve for 14 % YDH film. From measured capacitance and known thickness of film, the $\kappa$ value of the overall film is calculated to be ~16. The C-V data also shows a hysteresis having an anti-clockwise direction and a shift towards positive bias which is indicative of the presence of the negative charges trapped in the gate oxide [$^{52, 53}$]. This might be related to oxygen vacancies or interstitial oxygen defects [$^{54, 55}$] induced by the yttrium atoms. The trapped charge density was estimated to be about $4.5 \times 10^{12}$ cm$^{-2}$ [$^{52}$]. This is of the similar order as reported by Rauwel et al [$^{42}$] for their as-deposited YDH films. However, it is higher than the values for their films annealed in NH$_3$ at 900 ºC indicating that annealing could further lead to optimal electrical properties. Current-voltage measurements indicated low leakage current densities of below $10^{-5}$ A cm$^{-2}$ measured at gate bias voltage of 1 V. The leakage current level increases slightly with the increasing yttrium dopant from $10^{-6}$ A cm$^{-2}$ (pure hafnia) to $10^{-5}$ A cm$^{-2}$ (50% yttria doping); the leakage current level of the optimal 14 % YDH film is $5\times10^{-6}$ A cm$^{-2}$ at a bias voltage of +1 V.
Figure 24. (a) C-V and (inset) I-V curve for 14% yttrium-doped HfO$_2$ films. (b) The measured dielectric constant values of the nano-composite YDH film for different yttrium content after annealing at 800 °C. The thickness of the films is same as in the case of Figure 21.
Relative permittivity values for annealed YDH as calculated from the C-V measurements are plotted in Figure 24 (b). The relative permittivity of the atomic layer deposited HfO₂ and Y₂O₃ films are 9 and 6.6, respectively, as is indicated by the endpoints in Figure 24 (b). Interestingly, when HfO₂ films are doped with increasing amount of yttrium, the relative permittivity of the annealed YDH film is observed to increase and the values are higher than both pure HfO₂ and Y₂O₃. The YDH films achieve a maximum relative permittivity of 16 corresponding to the 14 % Y in terms of ALD cycle ratio. From the GIXRD results discussed earlier, this increase in the permittivity can be attributed to the phase transformation of the HfO₂ to the cubic polymorph, which is known to have a higher permittivity than amorphous and monoclinic phases.[³⁹] It should be also noted that the measured permittivity here corresponds to the entire dielectric stack comprising the yttrium-doped HfO₂ films together with the thin interfacial film. TEM images (Figures 23(b) and 23(c)) indicate the presence of a 1.5-2.5 nm thick interfacial layer. Based on this information, the corrected dielectric constant values for the YDH layer may be calculated by modeling the film structure as two capacitors (i.e. the YDH layer and the interfacial layers) in series. The corrected dielectric constant value for the 14% YDH film would then be about 21-23. Yang et al reported a dielectric value of 32 for YDH (grown by MBE) films without the presence of any interfacial layer.[⁴⁴] The yttrium percentage range required for achieving the maximum relative permittivity differs slightly from the reported values [¹⁸, ⁴²-⁴⁴]. But, the effect of addition of yttrium on the overall dielectric constant of the YDH film follows the same trend — the overall permittivity of YDH films increases with increasing yttrium content resulting in stabilized cubic HfO₂ structure and starts to decrease beyond this composition.
4.1.4. **Summary**

Yttrium-doped hafnium oxide thin films were deposited on silicon by atomic layer deposition using new yttrium precursor tris(ethylcyclopentadienyl) yttrium. Higher permittivity cubic-HfO$_2$ phase could be obtained when the yttrium content, as defined by the Y$_2$O$_3$ cycle ratio in the sequential ALD process, was 2.5% or more. The cubic HfO$_2$ stabilized by incorporation of 14 % yttrium doping had the highest dielectric constant ($\kappa$=21 - 23) with the leakage current of $10^{-5}$ A cm$^{-2}$ measured at gate bias voltage of 1 V. The controlled doping of Y$_2$O$_3$ in HfO$_2$ using atomic layer deposition significantly enhances the dielectric property of the film which can potentially lead to viable means of improving the performance of future CMOS gate oxides and DRAM capacitors. Identification of a good barrier layer could further help in achieving high permittivity in gate stack structures deposited by atomic layer deposition.
4.2. **Investigation of Surface Sputtering and Post Annealing Effects on Atomic Layer Deposited HfO$_2$ and TiO$_2$**

### 4.2.1. Introduction

Atomic layer deposition (ALD) has gained wide acceptance as robust means for depositing thin films because of its precise film thickness control, conformal growth on complex structures, low growth temperature, and low pinhole density [56-58]. All these advantages have made ALD attractive for ultrathin and/or highly conformal applications, such as gate insulator of metal oxide semiconductor field effect transistors and capacitor dielectric of dynamic random access memories [7, 59]. So far, many candidate gate dielectric materials for the replacement of SiO$_2$ have been studied such as Ta$_2$O$_5$, TiO$_2$, Al$_2$O$_3$, Y$_2$O$_3$, ZrO$_2$ and HfO$_2$. From all these materials, HfO$_2$ and TiO$_2$ seem to be promising candidates due to their favorable properties. For instance, the reported dielectric constant of HfO$_2$ and TiO$_2$ could be 15-30 and 7-80 or even higher [60, 61]. The large variation in dielectric constants of both HfO$_2$ and TiO$_2$ has been attributed to differences in film thickness, impurities in the film such as carbon, and structural phase of the deposited material after high temperature annealing [62].

Carbon contamination in dielectric films is always a concern for semiconductor manufacturing. So far, proposed methods for film surface cleaning from carbon contaminants include Ar$^+$ sputtering [63], VUV excimer lamp [64], and microwave oxygen plasma [65]. From all these methods, Ar$^+$ sputtering seems to be very effective means to clean the surface; however, for certain materials, it may also alter the material composition. The carbon impurity in the bulk film can be minimized by optimizing the
deposition process such as controlling the proper temperature and pressure range and allowing sufficient purging time between each reaction cycle. In this study, optimization of the ALD process is reported in detail with focus on the Ar+ surface sputtering and post-deposition annealing effects on the composition of the film, chemical bonding, morphology and structure [66].

4.2.2. **Experimentation**

HfO₂ and TiO₂ thin films were deposited using tetrakis (diethylamino) hafnium (TDEAH) and tetrakis (diethylamino) titanium (TDEAT) as metal precursors with H₂O as the oxidant. Prior to deposition, Si substrates (20 x 20 mm) were cleaned using Radio Corporation of America (RCA) standard cleaning (SC-1) to remove organic contaminants followed by 1% HF dip for 10 s to remove native oxide down to 1 nm as measured by spectral ellipsometry after cleaning. Each of two steps was followed by thorough de-ionized water rinsing and drying in N₂. Immediately after cleaning, the substrates were loaded into a hot wall ALD reactor to deposit HfO₂ or TiO₂ films. The metal precursors were contained in stainless steel vessels with the TDEAH reservoir kept at 66.7 °C and the TDEAT reservoir kept at 67.0 °C during deposition. Moisture was fed into the reactor via pulses of wet N₂ which resulted from a N₂ flow through a bubbler of water maintained at 0 °C. Further description of the ALD reactor along with other process parameters was reported in a previous ALD study [49].

In this study, the ALD film thickness was measured by spectral ellipsometer (J. A. Woollam Co., Inc., model M-44), after a sample is measured, a model is constructed to
describe this sample (the model is used to calculate the predicted response from Fresnel’s equation which describes the each material with thickness and optical constants). For each thickness determination, three measurements across the film were made with mean values representing the film thickness. In order to analyze the carbon impurity levels in the films, HfO2 and TiO2 layers deposited at different temperatures were probed with X-ray photoelectron spectrometer (Kratos AXIS-165) equipped with a monochromatic Al Kα (1486.6 eV) X-ray source operating at 15 kV and 10 mA. Ar+ sputtering was performed for 5 and 10 min (with sputtering rate of 0.1 nm/min) to remove the surface contaminant. Film structures before and after surface sputtering were compared by high-resolution X-ray photoelectron spectra (XPS) of the elements-of-interest using a pass energy of 20 eV, a step size of 0.1 eV and a dwell time of 200 ms. Semi-quantitative analysis of peak intensities was performed through spectral peak-fitting where peaks were subtracted from Shirley-type backgrounds and deconvoluted using Gaussian-Lorentzian peak shape functions. The binding energy scales of all XPS spectra were calibrated with reference to the adventitious carbon 1s position at 285 eV. In order to examine the post-deposition annealing effect on the film surface morphology and crystallinity, HfO2 and TiO2 films were annealed in N2 (99.996% ) for 5 min at 600 ºC and 1 atm in a preheated quartz horizontal furnace (Lindberg Blue STF) with a N2 flow rate of 40 sccm. Phase-shifting interferometry (PSI) was performed using a non-contact optical profiler (Wyko NT3300 system) to examine the surface roughness before and after annealing. A high resolution X-ray diffractometer (Philips X-pert) was used to obtain grazing incidence X-ray diffraction (GIXRD) spectra of HfO2 and TiO2 films. The GIXRD spectra were collected at a low angle of incidence at 0.7 ° with an overall
diffraction angle resolution of 0.15 °. The use of grazing incidence X-ray allowed high resolution diffraction patterns with enhanced sensitivity without interference of diffraction lines from the single crystalline Si (100) substrate. Before conducting Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements, 150 nm Al metal contacts were deposited on top of the HfO2 and TiO2 films by electron beam evaporation (Varian model # NRC3117). C-V and I-V measurements were performed at 100 kHz using Agilent 4980 equipped with MDC model 802B Mercury Probe, which was used in a front – front contact mode. C-V measurements were done over the voltage range of -2 to 2 V; frequencies from 1 to 100 KHz were used. Permeability was computed from the maximum capacitance. The area of metal contacts was $1.6 \times 10^{-3}$ cm².

4.2.3. Results and discussions

In order to ascertain that neither metal precursor decomposes in the reactor under deposition conditions, thermal decomposition tests were performed using the ALD reactor itself under deposition reaction conditions (figure 25). In these tests, a cleaned silicon substrate was placed in the ALD reactor and 30 cycles of metal precursor pulsing were performed without the use of any H2O oxidant over the temperature range of 50 – 275 °C for each precursor – TDEAT and TDEAH. As figure 25 shows, the silicon substrates were examined and showed no sign of decomposition residuals on a Si substrate up to 200 °C for either precursor. From 200 to 250 °C, very small amounts of residue were found indicating that both precursors probably started to decompose; after increasing the deposition temperature to 275 °C, there were pronounced residue left on the Si substrate suggesting decomposition of the metal precursors.
Figure 25. Thermal decomposition of TDEAH and TDEAT precursors in the ALD reactor
Carbon contamination of as-deposited films and films growth rates as functions of deposition temperatures are presented in figure 26. All films were deposited for 50 cycles with deposition temperatures below 250 ºC in order to avoid the decomposition of the precursors (figure 25). In our recently modified ALD reactor and bubbler system, the growth rate of HfO₂ reached a steady value of 0.12 nm/cycle at deposition temperatures 175 - 225 ºC, while within the same temperature range TiO₂ grew at about 0.10 nm/cycle.

The growth for both metal oxides exhibits higher growth rates at lower deposition temperatures likely due to excess condensation of precursor vapor on the substrate [67]. Carbon contamination of the films is also observed to be higher when the deposition temperature is below the temperature range in which constant-value growth rates are observed for both oxide films (figure 26). After 10 min of Ar⁺ sputtering, both HfO₂ and TiO₂ films are found to be carbon-free when deposition temperatures are within the range of 175 – 225 ºC; a small amount of carbon (less than 6%) is detected in both films deposited at 125 and 150 ºC (figure 26). Since 10 min of Ar⁺ sputtering has been found to be sufficient sputtering time to remove all surface contaminants, such carbon species likely come from the deposited film rather than the surface, and the source of carbon impurities in the film is likely condensed precursor vapor. The optimal deposition temperature range for both HfO₂ and TiO₂ carbon-free films is therefore determined to be 175 - 225 ºC.
Figure 26. Film carbon concentration (before and after 5 min Ar$^+$ sputtering) and growth rates of both oxides (inset) as a function of deposition temperature after 50 cycles. All films were deposited at 0.2 torr with 5 s precursor pulsing and 50 ms H$_2$O pulsing alternatively into the deposition chamber.
In order to study the surface sputtering effect on the film structure, element-of-interests were scanned for both films deposited at 200 °C and 50 cycles, with 5 minutes sputtering time. Figure 27 shows XPS core scans of Hf (a), O (b) and C (c) of HfO$_2$ samples before and after Ar surface sputtering. The core spectrum of Hf 4f before sputtering consisted of two components: 4f$_{5/2}$ at 19.1 eV and 4f$_{7/2}$ at 17.4 eV with the standard spin-orbital splitting (SOS) of 1.7 eV, as a reference of HfO$_2$ formation; peaks at lower binding energies were not observed, indicating absence of HfSi$_x$ formation during ALD [68]. After Ar$^+$ sputtering for 10 minutes, the Hf 4f peak positions remained the same, while peak intensity decreased due to the removal of HfO$_2$ layers. Oxygen 1s spectrum of the unsputtered HfO$_2$ film exhibited three peaks, which were assigned to Hf-O-Hf (529.7 eV), O-H (530.8 eV) and Si-O (531.7 eV) [69]; after sputtering, the O-H peak disappeared, indicating that O-H species resulted from surface absorbed water vapor (considering that there was no O-H group in the precursor ligands). Meanwhile, it was observed that the peak intensity of Hf-O-Hf decreased compared to the slightly increased Si-O one, suggesting that Si-O probably came from SiO$_2$ at the interface. A substantial amount of carbon was found in the unsputtered HfO$_2$ films. The strongest C 1s peak at 285 eV is designated as the adventitious carbon, the intermediate peak at 286 eV is assigned to C-OH, and the smallest peak at 289.2 eV is assigned to O=C-OH species [64, 70]. After sputtering, a tiny amount of adventitious carbon residues was found on the surface, and it could be removed by increasing the sputtering time to 10 minutes (figure 26).
Figure 27. XPS core spectra of Hf 4f (a), O 1s (b), C 1s (c) from 6 nm-thick HfO$_2$ before and after Ar$^+$ sputtering for 5 min
Figure 28 shows XPS core scans for Ti (a), O (b) and C (c) of TiO$_2$ samples before and after 5 minutes of Ar$^+$ sputtering. The unsputtered Ti 2p (Ti 2p$_{1/2}$ at 462.7 eV and Ti 2p$_{3/2}$ at 457.0 eV) with SOS of 5.7 eV was assigned to the Ti$^{4+}$ in TiO$_2$. Interestingly, after sputtering, the original Ti 2p$_{1/2}$ and Ti 2p$_{3/2}$ peaks decomposed into six primary peaks, and those peaks, based on earlier observation of XPS of TiO$_{2-x}$ [71, 72] were assigned to TiO$_2$ (at 463.8 eV and 458.6 eV), Ti$_2$O$_3$ (461.4 eV and 457.0 eV) and TiO (460.4 eV and 455.1 eV)—the newly formed Ti$^{2+}$ and Ti$^{3+}$ species will lead to the discrepancy and change in SOS of Ti 2p peaks. It is known that Ar$^+$ ion bombardment alters the chemical state and composition of some compounds such as TiO$_2$, NiO, Ta$_2$O$_3$, CuO, etc [73-75]. For instance, McCurdy, et al [76] found that TiO$_2$ reduced into different chemical states (Ti$_2$O$_3$ and TiO) depending on the time of Ar$^+$ sputtering or the temperature of post-deposition annealing. Hashimoto, et al [77] also reported that the appearance of Ti$^{2+}$ and Ti$^{3+}$ in addition to Ti$^{4+}$ after ion bombardment at 2 kV (4 kV in this present report) and a sufficient sputtering time would result in an equilibrium state between the sputtered atoms and implanted ions. However, in all cited reports, there lacked an analysis of differentiation of Ti (at different chemical states) associated O; figure 28 (b) shows that the Ti-O-Ti peak (at 530.0 eV before sputtering) deconvoluted into three peaks assigned to oxygen in those titanium suboxides next to the Si-O peak at 531.8 eV, which was found to slightly shift to higher binding energy by 0.3 eV compared with the Si-O peak in the unsputtered film. The O-H species from the unsputtered TiO$_2$ (530.5 eV) was, again, no longer observed after sputtering. The amount of carbon was largely reduced to less than 4% after sputtering with the removal of C-OH and O=C-OH species, but there showed two peaks at lower binding energies of the
adventitious carbon peak, which could be assigned to newly formed Ti-carbon (TiCₙ) species [78] after sputtering; those species might have resulted from the redeposition of sputtered Ti and carbon atoms (all these carbon species would be eventually removed after 10 minutes sputtering). Based on the XPS results, a preferential sputtering of O over Ti, with atomic ratio O/Ti decreasing from 2.5 to 1.5 after sputtering was observed, while such preferential sputtering was not found in ALD HfO₂ films.
Figure 28. XPS core spectra of Ti 2p (a), O 1s (b), C 1s (c) from 6 nm-thick TiO$_2$ before and after Ar$^+$ sputtering for 5 min.
The surface roughness of both as-deposited and post-annealed films is important because it affects shifts in electronic energy levels and may degrade electrical characteristics [79]. Surface morphology could also reveal crystalline phase formation. From phase-shift interferometry calibration of 28 nm-thick as-deposited TiO$_2$ and HfO$_2$ (figures 29a and 29c), both as-deposited films exhibited smooth surface with RMS (root mean square) roughness of about 0.22 nm for HfO$_2$ and 0.34 nm for TiO$_2$. Upon annealing at 600 °C, film surfaces become rougher with increased vertical spikes and the RMS roughness values were 0.93 nm for annealed HfO$_2$ and 0.97 nm for annealed TiO$_2$ (figure 26b and 26d, respectively).
Figure 29. PSI surface morphology of HfO$_2$ and TiO$_2$ before and after annealing at 600 °C in N$_2$ for 5 min
GIXRD graphs of as-deposited HfO$_2$ (inset of figure 30(a)) and as-deposited TiO$_2$ (inset of figure 30(b)), showed no diffraction peaks for two-theta degree of 20 - 40 therefore indicating the amorphous nature of the as-deposited HfO$_2$ and TiO$_2$ films; this corresponded to the rather smooth film surface with small RMS roughness probed with PSI and reported above. Upon annealing, HfO$_2$ crystallized into the monoclinic structure while TiO$_2$ crystallized into the anatase structure, albeit to a smaller extent, and that corresponded to the surface roughening process for both films resulting from post annealing (figure 29).
Figure 30. GIXRD diffractograms of 28 nm-thick HfO$_2$(a) and 20 nm-thick TiO$_2$ (b) films annealed at 600$^\circ$C for 5 min; insets include diffractograms of as-deposited HfO$_2$ (a) and TiO$_2$ (b). The grazing incidence angle is fixed at 0.7$^\circ$. 
C-V measurements were performed over the voltage range of -2 to +2 V at 100 kHz, and the corresponding I-V measurements were performed over the voltage range of 0 to 5 V at 100 kHz, (figures 31a and 31b, respectively). Dielectric constants of deposited films and interfacial layer were computed from the maximum capacitance observed in the accumulation region of C-V plots. From the measured thicknesses by spectral ellipsometry and maximum capacitances in the C-V plots, the film dielectric constant values were calculated (after correction for 1 nm of interfacial silicon oxide) to be 35 for TiO₂ and 12 for HfO₂; the corresponding equivalent oxide thickness (EOT) values were 1.6 nm for TiO₂ and 3.6 nm for HfO₂. It is noted that both dielectric constants were lower than other reported values of TiO₂ and HfO₂ likely because the measured samples were as-deposited and amorphous without any post-deposition treatments such as forming gas or high temperature annealing which could enhance dielectric properties and result in crystalline phases with higher dielectric constants [61, 62]. From I-V plots in the insets of figures 31(a) and 31(b), the leakage current density steeply increased when the applied voltage increased from 0 V to 1.6 V for HfO₂ and to 1 V for TiO₂ with incremental increases when the applied voltage was further increased to 5 V. The leakage current densities at the applied 1 V were 1.1x10⁻⁶ A/cm² for HfO₂ and 1.5x10⁻⁵ A/cm² for TiO₂. The measured leakage current densities of TiO₂ were four magnitudes lower than that of SiO₂ at a similar EOT level [80].
Figure 31. C-V and I-V curves (in insets) for 13 nm-thick as-deposited HfO$_2$ (a) and TiO$_2$ (b) films at 100 kHz.
4.2.4. **Summary**

In this work, HfO2 and TiO2 were successfully synthesized by atomic layer deposition with TDEAH, TDEAT, and H2O as oxidant. XPS results from about 6 nm-thick HfO2 and TiO2 films showed that all films had negligible carbon contamination after 10 minutes Ar+ surface sputtering when the deposition temperature was in the range of 175 - 225 °C - both films were found to grow at steady growth rates within this temperature range. Preferential sputtering of O over Ti was observed to result in the transition of Ti 4+ into Ti 2+ and Ti 3+ for TiO2 films, while such a transition did not occur for Hf 4+ (HfO2 films). As-deposited HfO2 and TiO2 films had smooth surface morphology which became rougher after annealing at 600 °C for 5 minutes in N2. Based on GIXRD analyses, the roughened surface and film crystallization are correlated with the post deposition annealing process. From C-V measurements, the dielectric constants were determined to be 12 and 35 for HfO2 and TiO2, respectively, with corresponding EOT values of 1.6 nm (TiO2) and 3.6 nm (HfO2) (for samples prepared and analyzed at the aforementioned conditions). Although HfO2 films exhibited a lower dielectric constant and bigger EOT value than that of TiO2, they appeared to be superior to TiO2 films in terms of confining leakage current density, i.e., with one order of magnitude lower values that that of TiO2 at 1 V. Both ALD HfO2 and TiO2 films exhibited promising dielectric properties for future gate oxides in CMOS applications.
4.3. Atomic Layer Deposition of HfO$_2$, TiO$_2$ and Hf$_x$Ti$_{1-x}$O$_2$ using metal (diethylamino) precursors and H$_2$O

4.3.1. Introduction

Structural and interfacial studies of ultrathin, high dielectric constant (κ) films during high temperature fabrication processes are critical to the continuous scaling of microelectronic devices. In particular, these materials are of great importance for the gate insulator of metal oxide semiconductor field effect transistors and the capacitor dielectric of dynamic random access memories [59, 81]. So far, many candidate materials such as Ta$_2$O$_5$, TiO$_2$, Al$_2$O$_3$, Y$_2$O$_3$, ZrO$_2$ and HfO$_2$ have been studied for the replacement of SiO$_2$ [82]. From all these materials, HfO$_2$ and TiO$_2$ seem to be promising candidates due to their favorable properties. HfO$_2$ is known to have relatively good thermal stability and compatibility with the Si substrate, and it has a dielectric constant of 15 – 30 with a large band gap (5.7 eV) [60, 83, 84]. TiO$_2$ is even more favorable in terms of its dielectric constant which is 80 or higher [85]; however, it has a rather small band gap (3.1 eV) [86] which could result in more leakage current than that of HfO$_2$. The reported crystallization temperature of each of these two materials has been reported to be as low as ~ 550 °C [87, 88].

The earliest atomic layer deposition (ALD) of HfO$_2$ from tetrakis (diethylamino) hafnium (TDEAH) and H$_2$O was published by Deshpande et. al. with a growth rate of ~ 0.13 nm/cycle at 300 °C.[11] Titanium tetrachloride (TiCl$_4$) and titanium isopropoxide (TTIP) have typically been used as metal precursors in the ALD of TiO$_2$ films, with water being the oxidant [89-93]. Reported growth rates in these systems have been 0.03
nm/cycle or less. Our earlier ALD studies with other homoleptic metal precursors having the diethylamino ligand, such as TDEAH and tris (diethylamino) aluminum, have resulted in broad ALD temperature windows and rather high growth rates [87, 94, 95] Such results prompted interest in examining the suitability of tetrakis (diethylamino) titanium (TDEAT) as a precursor for the ALD of TiO$_2$ and Hf$_x$Ti$_{1-x}$O$_2$ and in studying process – structure – property relationships of the resulting thin films.

In previous studies, Hf$_x$Ti$_{1-x}$O$_2$ films were mainly grown with physical or chemical vapor deposition. For instance, Rhee et al. [96] studied a HfO$_2$/TiO$_2$ bilayer structure formed by sputtering, and the resulted HfO$_2$/TiO$_2$ transistor had a κ value of 36 with equivalent oxide thickness (EOT) of 0.8 nm. Li et al. [97] used Hf(C$_4$H$_9$O)$_4$ and Ti(NO$_3$)$_4$ to codeposit Hf$_x$Ti$_{1-x}$O$_2$, with x between 0.3 and 0.5; the dielectric constant of the resulting films was reported to linearly increase with increasing Ti content in this composition range, while the smallest reported EOT was 1.4 nm. Recently, Shao et al. [98] studied Hf$_x$Ti$_{1-x}$O$_2$ by chemical vapor deposition from Hf–Ti composite nitrates that were formed from HfCl$_4$ and TiCl$_4$ precursors, and they found that the Hf$_x$Ti$_{1-x}$O$_2$ had a low EOT of 1.3 nm, when x = 0.09, with a rather high leakage current density of 0.61 A/cm$^2$ at 1 V bias due to the high content of Ti in the film.

Earlier reports on atomic layer deposition of Hf$_x$Ti$_{1-x}$O$_2$ structures showed variation of electrical properties depending on the precursors and annealing conditions used; for example, Kukli et al. used HfCl$_4$ and Ti(OC$_2$H$_5$)$_4$ precursors and observed a film permittivity of 51 at 1 MHz with a leakage current of 8.6x10$^{-5}$ A/cm$^2$ at 1 V bias.
using a Ru bottom electrode [52]. Triyoso et al. [92, 93] used HfCl$_4$ and TiCl$_4$ to prepare Hf$_x$Ti$_{1-x}$O$_2$ films on HfO$_2$ (10 nm-thick)/SiO$_2$ (chemical oxide)/Si substrates with different atomic ratios of Hf and Ti; a dielectric constant as high as 39 was reported yielding a capacitance equivalent thickness (CET) of 1.4 nm and a leakage current density of $10^{-2}$ A/cm$^2$ at 1 V bias. Popovici, et. al. [99] reported Hf$_x$Ti$_{1-x}$O$_2$ film deposition on SiO$_2$ (1 nm-thick O$_3$/H$_2$O oxidation)/Si and Pt (85 nm-thick)/TiO$_2$ (10 nm-thick rutile)/Si substrates by ALD using the same chloride metal precursors as Triyoso, et. al. [92, 93] they observed an EOT of $\sim$ 1 nm and a leakage current density of $\sim$ $10^{-7}$ A/cm$^2$ at 1 V, after annealing in O$_2$ ambient.

In this study, ALD growth kinetics of TiO$_2$ using TDEAT precursor is investigated and reported along with the co-ALD of TiO$_2$ and HfO$_2$ to form Hf$_x$Ti$_{1-x}$O$_2$ films on silicon substrates with variable amounts of Hf and Ti; identical ligand precursors are used in the deposition of these films, i.e., TDEAT and TDEAH. The composite films are analyzed and discussed in terms of structure and interfacial interactions as a function of composition to assess the influence of Ti on the properties of the resulting Hf$_x$Ti$_{1-x}$O$_2$ films.

4.3.2. Experimentation

HfO$_2$ and TiO$_2$ thin films were deposited using TDEAH (Air Liquide) and TDEAT (Air Liquide) as metal precursors and H$_2$O as the oxidant. Prior to deposition, the Si substrates (20x20 mm) were cleaned using Radio Corporation of America (RCA) standard cleaning (SC-1) to remove organic contaminants followed by 2% HF dip for 20
s to remove native oxide down to ~ 4 Å as measured by spectral ellipsometry. Each of these two steps was followed by thorough deionized water rinsing and drying in N₂. Immediately after cleaning, the substrates were loaded into the hot wall ALD reactor to deposit HfO₂, TiO₂ and HfₓTi₁−ₓO₂ composite films. The metal precursors were in stainless steel vessels; during deposition, the TDEAH reservoir was kept at 65 °C and the TDEAT reservoir at 67 °C. Precursor decomposition characteristics under the deposition conditions used here were probed with a cleaned silicon substrate that was placed in the ALD reactor followed by 30 cycles of either TDEAT or TDEAH metal precursor without the use of H₂O oxidant, over the temperature range of 150 – 275 °C. Afterwards, the silicon samples were analyzed and showed no decomposition residual on the Si substrate up to 250 °C for either precursor; precursor decomposition was found to become significant at 275 °C. These findings suggested precursor stability within the reactor up to at least 250 °C.

In the actual ALD studies, moisture was supplied to the reactor through pulses of wet N₂ formed by a continuous flow of N₂ through a bubbler of water maintained at 0 °C. Further description of the ALD reactor along with other process parameters was reported elsewhere [⁴⁹]. In the case of HfₓTi₁−ₓO₂ deposition, the TDEAH/H₂O and TDEAT/H₂O ALD cycles were used in the ratios of 1:5, 1:3, 1:1, 3:1, and 5:1 in order to vary the composition of the film over a wide range; these cycle ratios were repeated until a desired film thickness was obtained.
The ALD film thickness was measured with a spectral ellipsometer (J. A. Woollam Co., Inc., model M-44); for each thickness determination, three measurements across the film were done with mean values representing the film thickness and standard deviation indicating uniformity of the film thickness. For studies on possible thermally induced phase transitions and interfacial reactions, the ALD films were annealed in 4000 sccm N₂ (99.996%) for 5 min at a temperature between 600 and 1000 ºC at 1 atm in a preheated quartz horizontal furnace (Lindberg Blue STF); the temperature in the furnace was maintained within ±2 ºC. Films analyzed with X-ray photoelectron spectroscopy (XPS) were annealed in air at 600 ºC. The composition and interfacial structure were probed with an XP spectrometer (Kratos AXIS-165) equipped with a monochromatic Al Kα (1486.6 eV) X-ray source operating at 15 kV and 10 mA. All XP spectra were collected at zero-degree take-off angle using an eight-channeltron concentric hemispherical analyzer. High-resolution spectra of the elements-of-interest were collected using pass energy of 20 eV, step size of 0.1 eV and dwell time of 200 ms. Semi-quantitative analysis of peak intensities was performed through spectral peak-fitting where peaks were subtracted from Shirley-type backgrounds and deconvoluted using Gaussian-Lorentzian peak shape functions (software XPS PEAK Version 4.1). The binding energy scales of all XPS spectra were calibrated with reference to the adventitious carbon 1s position at 285 eV. Phase-shifting interferometry (PSI) was performed using a non-contact optical profiler (Wyko NT3300 system) to study surface morphology to within 0.1 nm vertical resolution. A high resolution X-ray diffractometer (Philips X-pert) was used to obtain grazing incidence X-ray diffraction (GIXRD) spectra of HfO₂, TiO₂ and HfₓTi₁₋ₓO₂ films. The GIXRD spectra were collected at 0.7° angle of
incidence with an overall diffraction angle (2θ) resolution of 0.15°. The use of grazing
incidence X-ray allowed high resolution diffraction patterns with enhanced sensitivity for
thin films without diffraction line interference from the single crystal Si (100) substrate.

4.3.3. **Results and discussion**

A. **ALD of HfO$_2$, TiO$_2$ and Hf$_x$Ti$_{1-x}$O$_2$ films**

   a. **Precursor dosage**

   Figures 1a and 1b show the effect of precursor pulse time on the growth rates of
HfO$_2$ and TiO$_2$, respectively, deposited at 200 ºC with the error bars representing
standard derivations of film thickness measurement of three points across the substrate
surface. During the ALD process, moisture was pulsed into the reactor for 50 ms
followed by 10 s N$_2$ purging. The amount of precursor dosage was controlled with the
duration of each precursor pulse. The growth rates were found to increase with increasing
precursor pulse time and saturate after 5 s for the hafnium precursor and 3 s for the
titanium precursor (Figure 32). No further change of the growth rate was found with
further increases of the pulse time.
Figure 32. Growth rate of HfO$_2$ (a) and TiO$_2$ (b) thin films using TDEAH/TDEAT and H$_2$O on silicon substrates as a function of precursor dosage (pulsing time). The reactor temperature was 200 °C and depositions were carried out at a constant precursor temperatures of 65 °C (TDEAH) and 67 °C (TDEAT) with a water pulse time of 50 ms. The vertical error bars indicate film uniformity across the whole sample.
b. ALD temperature window

The temperature dependence of growth rates is shown in Figure 33. The higher growth rates at lower temperatures often result from multi-layer condensation of precursor vapor on the substrate, while the lower growth rates at higher temperatures can be attributed to lower adsorption of the precursor on the surface [67]. The region where the deposition rate is independent of the substrate temperature is an optimal temperature window for ALD of each metal oxide. The upper limit of reaction temperature studied was 275 ºC which was the temperature at which the metal precursors were found to decompose within the ALD reactor, as it was discussed in the previous section. From Figure 33, the ALD temperature window for HfO$_2$ is 175 - 250 ºC and for TiO$_2$ 150 - 250 ºC. The data indicates a slight decrease of TiO$_2$ growth rates when the deposition temperature is higher than 200 ºC, and this may be due to a small loss of the reactive surface groups [100]. In this study, the deposition temperature for each metal oxide as well as Hf$_x$Ti$_{1-x}$O$_2$ was kept at 200 ºC.
Figure 33. Growth rate of HfO$_2$ (a) and TiO$_2$ (b) deposited by using TDEAH/TDEAT and H$_2$O on silicon substrates as a function of reaction temperature. Other deposition conditions were same as those in Figure 32. ALD temperature windows for HfO$_2$ and TiO$_2$ overlap between 175 and 250 $^\circ$C.
c. Deposition rate

Figure 34a shows the thickness of ALD HfO$_2$ and TiO$_2$ films measured after different number of cycles. The film thickness increases linearly with increasing number of cycles and from the slopes of linear regression analysis of the data the calculated growth rates are $\sim 0.12$ nm/cycle for HfO$_2$ and $\sim 0.06$ nm/cycle for TiO$_2$. The growth rate of HfO$_2$ is consistent with that reported by Deshpande et. al. [11] and Katamreddy et. al. [44, 94, 101] using the same hafnium precursor and H$_2$O as the oxidant in a different system. The thermal ALD rate of TiO$_2$ is higher than that reported with other Ti precursors, namely TTIP and TiCl$_4$, and water as oxidant [89-92]; on the other hand, even higher growth rates have been reported with the use of oxygen plasma [71]. The self-limiting nature of the ALD process is also manifested by the high degree of uniformity of the film thickness across the entire substrate area (Figures 32 – 34).
Figure 34. Thickness of HfO$_2$ and TiO$_2$ deposited by using TDEAH/TDEAT and H$_2$O on silicon substrates as a function of the number of cycles (a). The linear relationship between film thicknesses and reaction cycles resulted in 0.12 nm/cycle for HfO$_2$ and 0.06 nm/cycle for TiO$_2$. The deposition rates of Hf$_x$Ti$_{1-x}$O$_2$ as a function of Hf composition are shown in (b). Other deposition conditions were the same as those in Figure 32.
The growth rate of Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} films is found to increase linearly with increasing HfO\textsubscript{2} content in the film (Figure 24b) in a manner consistent with growth rates determined from individual metal oxides films. Thus, comparison of the data in Figures 34a and 34b indicates that film growth rates are independent of the metal oxide surface. That is, the deposition rate of HfO\textsubscript{2} on HfO\textsubscript{2} is similar to that of HfO\textsubscript{2} on TiO\textsubscript{2} and the deposition rate of TiO\textsubscript{2} on TiO\textsubscript{2} is similar to that of TiO\textsubscript{2} on HfO\textsubscript{2}.

B. **Effect of post-deposition annealing on Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2}/Si interfacial structures**

The XPS spectra of Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} films with ALD cycle ratio of [TDEAH/H\textsubscript{2}O]:[TDEAT/H\textsubscript{2}O] = 1:3 are shown in Figure 35. The locations of the peaks of each element in this study as well as in previous studies are presented in Table II. Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} films with different ALD cycle ratios generally have similar peak shapes and locations of XPS spectral features. The spectra in Figures 35a and 35c consist of two peaks corresponding to the Hf 4f\textsubscript{5/2} and 4f\textsubscript{7/2} components of as-deposited and post-deposition annealed (PDA) Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} film at 600 ºC in air for 5 min, respectively. Peaks indicative of hafnium silicide at lower binding energies are not observed [60, 68, 102]. The core-level spectra of both as-deposited and PDA Ti in Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} films show the two peaks corresponding to Ti 2p\textsubscript{1/2} and Ti 2p\textsubscript{3/2} (Figures 35b and 35d, respectively) which are consistent with Ti\textsuperscript{4+}, while no peaks are observed at lower binding energies indicating the absence of silicide formation [48, 103-105].
Figure 35. Hf 4f (a), Ti 2p (b), O 1s (c) and Si 2p (f) core scans of as-deposited Hf$_x$Ti$_{1-x}$O$_2$ with ALD cycle ratio of HfO$_2$:TiO$_2$ = 1:3. Hf 4f (c), Ti 2p (d), O 1s (g) and Si 2p (h) core scans of post-deposition annealed Hf$_x$Ti$_{1-x}$O$_2$ films in air at 600 °C for 5 min. The film thickness is ~ 5 nm; other film growth conditions are the same as those in Figure 32.
In order to further understand the O bonding in the films, O 1s XP spectra of as-deposited and PDA films were analyzed (Figures 35e and 35g, respectively). The O 1s spectrum of as-deposited HfₓTi₁₋ₓO₂ films reveals two peaks: the dominant one is consistent with a M-O-M bonding (M refers to Hf or Ti) [69, 76], while a small shoulder peak at 531 eV appears after spectral peak deconvolution, and this is likely due to O-H from absorbed moisture on the surface [106]; however M-O-Si bonding appears near this same band energy and therefore deciphering between O-H and M-O-Si may not be done from O 1s spectra alone [76, 79, 107].
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The Si 2p XP spectra from both as-deposited and PDA Hf$_x$Ti$_{1-x}$O$_2$ films are shown in Figures 35f and 35h, respectively. The as-deposited film (Figure 35f) shows only elemental silicon without evidence of M-O-Si. Therefore, the small O 1s shoulder peak at 531 eV in Figure 35e can be attributed to O-H. After annealing at 600 °C, the XPS of Si 2p (Figure 4h) indicates formation of M-O-Si at intermediate binding energy and O-Si-O at the highest binding energy [107] which are in agreement with the assignments of silicate and silicon oxide in the O 1s spectrum (Figure 35g) [36], since moisture would have desorbed from the surface at this annealing temperature. Also, because the film is 5 nm-thick, the silicon oxide is likely at the film-substrate interface.

C. Film composition tunability with ALD

For the control of the composition of Hf$_x$Ti$_{1-x}$O$_2$ films, a number of depositions were carried out with variable ALD cycle ratios of TDEAH/H$_2$O and TDEAT/H$_2$O. For example, when the ALD cycle ratio [HfO$_2$/ (TiO$_2$+HfO$_2$)] was equal to 50 %, one cycle of HfO$_2$ deposition alternated with one cycle of TiO$_2$ deposition. Figure 36 shows the effect of cycle ratio [HfO$_2$/ (TiO$_2$+HfO$_2$)] on the atomic composition of Hf$_x$Ti$_{1-x}$O$_2$ films 5 - 7 nm-thick as determined from XPS. The increase in the atomic ratio of Hf/(Hf+Ti) in Hf$_x$Ti$_{1-x}$O$_2$ with increasing ALD cycle ratio of [HfO$_2$/ (TiO$_2$+HfO$_2$)] indicated excellent tunability of the Hf$_x$Ti$_{1-x}$O$_2$ film composition with one-to-one Hf to Ti correspondence. This advantage of controlling nanofilm composition with ALD was also found and reported in our earlier work with HfO$_2$/Y$_2$O$_3$ nanostructures [87].
Figure 36. Hf,Ti$_{1-x}$O$_2$ film composition evaluated using XPS as a function of cycle ratio. Elemental compositions were calculated from quantitative analysis of the XPS spectra of the corresponding elements. Error bars represent the accuracy of XPS quantification, which is about 5% ($\pm$2.5%). Other conditions are similar to those in Figure 32.
D. **Surface morphology**

a. **As-deposited and post-annealed single metal oxide films**

Surface morphology of deposited films is important because it can significantly influence electronic energy levels and electrical characteristics [79]. Changes in surface morphology often indicate changes in underlining crystalline structures. Figures 37 and 38 show PSI images of 28 nm-thick films of both as-deposited and annealed HfO$_2$ and TiO$_2$, respectively. The as-deposited HfO$_2$ film (Figure 37a) is seen to be fairly flat with a root-mean-square (RMS) roughness of ~0.22 nm which is comparable to that of an undeposited Si substrate. The as-deposited TiO$_2$ film (Figure 38a) is found to be slightly rougher with an RMS of ~0.34 nm. Much higher surface roughness has been reported for TiO$_2$ deposited by CVD processes; for example, MOCVD TiO$_2$ using TTIP precursor resulted in films over 30 nm-thick with an RMS greater than 4 nm [108,109]. In another CVD study using TDEAT [110] and 7 nm-thick films, the RMS was reported to be ~1 nm. It is noted that those CVD studies on TiO$_2$ were done at a reaction temperature of 300 °C or higher, while in our study the temperature was 200 °C. Both reactor temperature and deposition process used could indeed be contributing factors to the higher roughness reported in the CVD of TiO$_2$ films.
Figure 37. PSI images of (a) as-deposited and annealed HfO$_2$, Ra: 0.17 nm, Rq: 0.22 nm, Rz: 2.2 nm; and (b) HfO$_2$ after post-deposition annealing at 600 °C in N$_2$ for 5 min, Ra: 0.72 nm, Rq: 0.93 nm, Rz: 9.2 nm; (Ra: Roughness Average; Rq: RMS Roughness; Rz: Max Profile Peak Height)
In this work, both HfO$_2$ and TiO$_2$ ALD film surfaces became rougher with visible clusters on the surface after annealing the resulting films at 600 °C in N$_2$ for 5 min (Figures 37b and 38b, respectively); their RMS almost tripled compared to that of as-deposited films, i.e., 0.93 nm for annealed HfO$_2$ and 0.99 nm for annealed TiO$_2$. This sharp increase in roughness is likely attributed to a structure phase transformation after annealing [86] that is apparently corroborated by GIXRD results (in later sections).
Figure 38. PSI images of (a) as-deposited and annealed TiO$_2$, Ra: 0.26 nm, Rq: 0.34 nm, Rz: 4.1 nm; and (b) TiO$_2$ after post-deposition annealing at 600 °C in N$_2$ for 5 min, Ra: 0.76 nm, Rq: 0.99 nm, Rz: 9.9 nm.
b. As-deposited and post-annealed Hf<sub>x</sub>Ti<sub>1-x</sub>O<sub>2</sub>

Figure 8 shows the surface morphology of Hf<sub>x</sub>Ti<sub>1-x</sub>O<sub>2</sub> films with the TDEAH/H<sub>2</sub>O to TDEAT/H<sub>2</sub>O cycle ratio of 3:1 for the as-deposited film (Figure 39a) and the post-deposition annealed ones at 800 and 1000 °C (Figures 39b and 39c, respectively). A large increase in the RMS surface roughness is observed only after annealing at 1000 °C. As-deposited Hf<sub>x</sub>Ti<sub>1-x</sub>O<sub>2</sub> films with an RMS of 0.28 nm (Figure 39a) are found to be as flat as as-deposited HfO<sub>2</sub> and TiO<sub>2</sub> films (Figures 37a and 38a). Hf<sub>x</sub>Ti<sub>1-x</sub>O<sub>2</sub> films deposited with the TDEAH/H<sub>2</sub>O to TDEAT/H<sub>2</sub>O cycle ratio of 3:1 were found to remain smooth with practically unchanged RMS of 0.34 nm after annealing at 800 °C (Figure 39b). However, when the PDA temperature increased to 1000 °C, the film started having an uneven surface morphology with visible agglomeration and film surface with needle-like lamella (Figure 39c); the RMS value was found to increase three-fold compared to that of films annealed at 800 °C. This is in contrast to HfO<sub>2</sub> and TiO<sub>2</sub> films that showed sharp increases in surface roughness at the much lower annealing temperature of 600 °C. The addition of Ti therefore effectively prevented roughening of the surface as well as likely structural phase transformation from post-deposition annealing up to at least 800 °C. Interestingly, Song and Takoudis reported that surface roughness of as-deposited TiO<sub>2</sub> was improved with the incorporation of a different dopant, i.e., Al<sub>2</sub>O<sub>3</sub>, at their conditions [110].
Figure 39. PSI images of as-deposited and annealed Hf$_x$Ti$_{1-x}$O$_2$ with [HfO$_2$/H$_2$O]:[TiO$_2$/H$_2$O]=3:1 (a) as-deposited, Ra: 0.22 nm, Rq: 0.28 nm, Rz: 3.4 nm; (b) Hf$_x$Ti$_{1-x}$O$_2$ after post-deposition annealing at 800 °C in N$_2$ for 5 min, Ra: 0.26 nm, Rq: 0.3 nm, Rz: 4.3 nm; and (c) Hf$_x$Ti$_{1-x}$O$_2$ after post-deposition annealing at 1000 °C in N$_2$ for 5 min, Ra: 0.95 nm, Rq: 1.2 nm, Rz: 8.9 nm.
E. **Effects of post-deposition annealing on film crystallinity**

a. Structure of HfO\textsubscript{2} and TiO\textsubscript{2} after post-deposition annealing

In earlier studies [50, 94], it was found that the incorporation of Al or Si increased the needed annealing temperature for crystallization of the resulting HfO\textsubscript{2}-based films. Incorporation of TiO\textsubscript{2} into HfO\textsubscript{2} was therefore investigated in this study.

GIXRD results of HfO\textsubscript{2} and TiO\textsubscript{2} films are shown in Figures 40 and 41, respectively. All films were 28 nm-thick as measured by spectroscopic ellipsometry; as-deposited (insets of Figures 40 and 41) and PDA films at 600 and 800 °C were studied. For both as-deposited HfO\textsubscript{2} and TiO\textsubscript{2} films, there were no noticeable diffractions peaks (insets of Figures 40 and 41, respectively) which therefore revealed amorphous structure in both material systems. However, upon annealing at 600 °C or higher temperature, pure HfO\textsubscript{2} and TiO\textsubscript{2} films appeared to crystallize into monoclinic and anatase structures, respectively, albeit the anatase peaks were considerably weaker. These results were in agreement with the PSI surface morphology studies in which surfaces became rougher with noticeable enlarged cluster size and a crystallization transformation likely induced by temperature annealing at 600 °C or higher.
Figure 40. GIXRD patterns of as-deposited and annealed HfO$_2$ as-deposited film (inset), and post-deposition annealed at 600 °C in N$_2$ for 5 min (a) and post-deposition annealed at 800 °C in N$_2$ for 5 min (b). All ALD conditions are the same with those in Figure 32. Monoclinic HfO$_2$ reference: PDF Card No. 00-040-1173.
Figure 41. GIXRD patterns of as-deposited and annealed TiO$_2$ as-deposited film (inset), post-deposition annealed at 600 °C in N$_2$ for 5 min (a), and post-deposition annealed at 800 °C in N$_2$ for 5 min (b). All ALD conditions are the same with those in Figure 32. Anatase TiO$_2$ reference: PDF Card No. 00-021-1272.
b. Crystalline structure of Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} upon annealing

HfO\textsubscript{2} – rich and TiO\textsubscript{2} – rich Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} 28 nm-thick films deposited with different [TDEAH/H\textsubscript{2}O]:[TDEAT/H\textsubscript{2}O] cycle ratios were found to remain amorphous after annealing in N\textsubscript{2} up to 800 °C for 5 min (insets of Figures 42 and 43, respectively). After annealing at 1000 °C, the hafnium-rich Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} films grown with cycle ratios [TDEAH/H\textsubscript{2}O]:[TDEAT/H\textsubscript{2}O] of 5:1, 3:1 and 1:1 (Figures 42a, 42b and 42c, respectively) showed only weak features of monoclinic HfO\textsubscript{2}, i.e., much less intense than those observed with pure HfO\textsubscript{2} films. The apparent monoclinic phase of the hafnium-rich Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2} film manifested itself at a much higher annealing temperature.
Figure 42. GIXRD patterns of 28-nm-thick Hf$_x$Ti$_{1-x}$O$_2$ films with [TDEAH/H$_2$O]:[TDEAT/H$_2$O] cycle ratios of 1:1 (a), 3:1(b) and 5:1 (c). Other ALD conditions are the same with those in Figure 1. The annealing temperature is 800 °C for the inset graph and 1000 °C for main graph. Monoclinic HfO$_2$ reference: same as in Figure 40.
Titanium-rich films deposited with [TDEAH/H$_2$O]:[TDEAT/H$_2$O] cycle ratios of 1:3 and 1:5 (Figures 43a and 43b, respectively) were mostly amorphous with trace amounts of orthorhombic HfTiO$_4$ phase present after annealing in N$_2$ at 1000 °C. Because of the low intensity of the observed diffraction features and the overlap of the different crystalline diffraction lines such as monoclinic HfO$_2$ (111) and orthorhombic HfTiO$_4$ (002) at the 2θ region of 32 - 33°, it was indeed hard to assert the formation of an orthorhombic phase. This is in contrast to the relatively high crystallinity of orthorhombic HfTiO$_4$ structure reported by Triyoso et. al. on HfO$_2$ (10 nm-thick)/SiO$_2$ (chemical oxide)/Si substrates [92, 16], which were also annealed at 500 °C in O$_2$ for 60 s or at 900 °C in N$_2$ for 60 s followed by a 5 s anneal at 1000 °C in N$_2$. Popovici, et. al. [99] also observed the orthorhombic phase of HfTiO$_4$ on (1 nm-thick O$_3$/H$_2$O oxidation)/Si and Pt (85 nm-thick)/TiO$_2$ (10 nm-thick rutile)/Si surfaces with 34 - 60 % Hf incorporation after annealing at 700 °C in N$_2$; in both studies, the precursors were chlorides and the deposition temperature was 300°C. Therefore, there are several possible factors which may have contributed to the different crystallization results in those studies such as differences of the nature of the substrate surface and surface preparation (likely the most important ones), annealing methods, ALD reaction temperature, and metal precursors used. Understanding how these factors influence film crystallization needs further studies in order to gain even greater deposition control of the resulting films not only in terms of atomic dimensionality and composition but structure as well; this could have significant consequences on the electrical properties of the resulting nanostructures.
Figure 43. GIXRD patterns of 28-nm-thick Ti-rich Hf_{x}Ti_{1-x}O_{2} films with [TDEAH/H_{2}O]: [TDEAT/H_{2}O] cycle ratios of 1:3 (a), and 1:5 (b). Other ALD conditions are the same with those in Figure 1. The annealing temperature is 800 °C for the inset graph and 1000 °C for main graph. Orthorhombic HfTi04 reference: PDF Card No. 04-002-5555
4.3.4. **Summary**

TDEAT and TDEAH with H2O were used for the ALD of HfO2, TiO2 and HfxTi1-xO2 films on Si. The growth rates of HfO2 and TiO2 with temperature-optimized ALD conditions were found to be 0.12 and 0.06 nm/cycle, respectively, and they remained unchanged during HfxTi1-xO2 film formation. TDEAT and TDEAH were found to be suitable and effective precursors for HfxTi1-xO2 deposition within the ALD temperature window of 175 - 250 ºC. XPS results suggested the formation of silicates and silicon oxide in ALD HfxTi1-xO2 films, after annealing in air for 5 min. The atomic ratio for Hf/Ti in HfxTi1-xO2 films was found to increase monotonically with increasing [TDEAH/H2O]: [TDEAT/H2O] cycle ratios and this demonstrated an excellent tunability of the HfxTi1-xO2 composition in these films. All non-annealed films exhibited smooth surfaces with small RMS values as probed by PSI; however, after annealing at 600 ºC, TiO2 and HfO2 surfaces became rougher along with visible nucleation which could be indicative of crystallization. HfxTi1-xO2 films remained smooth after post-deposition annealing up to 800 ºC, and they started to become rougher with a needle-like structure after annealing in N2 at 1000 ºC for 5 min. These findings correlated satisfactorily with PDA induced crystallization probed with GIXRD whereby the crystallization temperature for HfO2 and TiO2 was 600 ºC (or lower), while HfxTi1-xO2 films remained practically amorphous after annealing up to about 1000 ºC, at the conditions studied.
4.4. Selective Atomic Layer Deposition of HfO$_2$ on Copper Patterned Silicon Substrate

4.4.1. Introduction

Atomic layer deposition (ALD) is a powerful means of fabricating nanoscale features in three dimensional structures which have importance in a wide range of applications such as solid oxide fuel cells \cite{98,111}, memory storage \cite{112,113}, and chemical sensors \cite{114}. In the fabrication of semiconductor devices, ALD has been used extensively to create gate oxide layers in field effect transistors, dielectric layers in capacitive memory cells, and diffusion barrier layers for copper interconnects of semiconductor logic processing units. In all these applications, patterning of the ALD film is required for device functionality. The patterning can be done subtractively by global deposition followed by selective removal of the film or by selective atomic layer deposition (SALD).

SALD is a more efficient process in that it eliminates the selective removal steps often involving combinations of chemical etch with expensive reagents and photolithography. For this reason, there is a lot of interest in selective deposition techniques. The most common approach of SALD is to provide a molecular mask over selected non-deposited areas. In recent years several self assembled monolayer materials have been effective in preventing deposition \cite{20}; specifically for the ALD of HfO$_2$, several self-assembled monolayers (SAMs) have been evaluated \cite{21}. However, SAMs typically have long assembly times of the order of hours before impervious layer is established to fully prevent deposition and require removal after deposition. An alternate and more efficient approach to SALD is to take advantage of the different materials at
the surface having different nucleation times for film growth by ALD. For example, the ALD of HfO$_2$ on bare silicon exhibits an inhibited growth due to lack of hydroxyl surface sites for ALD; however, in this case the nucleation time is quite short and on the order of only a couple of ALD cycles [22]. Nonetheless, surprisingly this surface dependence for different materials has not been evaluated at length despite the useful benefit especially as deposited layers approach a few nanometers thickness.

4.4.2. **Experimentation**

In these experiments, about 2 cm x 2 cm sections of silicon (100) substrates were partially coated with copper using E-beam Evaporation (Varian model # NRC3117). The E-beam was provided with a 10 kV voltage having 175 mA current resulting in 0.24 nm/sec copper deposition. In this manner, ~ 200 nm-thick copper coating was deposited on the patterned substrates over a portion of the silicon substrate whereas the other portion (about one-half of the silicon substrate) was masked during the evaporation process in order to prepare the partially copper coated silicon substrates. Both copper and silicon portions of the substrates have oxide on the surface and the thicknesses of these oxides were measured using a spectral ellipsometer (Woollam M-44). Immediately after evaporation, the surface oxide on copper was about 0.5 nm with no noticeable change over a few hours interval, and 1.5 nm native oxide on silicon. To minimize any additional oxidation of the copper surface, the ALD of HfO$_2$ was done within one hour after copper partially coated the silicon substrate. After ALD, samples were analyzed by spectral ellipsometry and x-ray photoelectron spectroscopy (XPS, Kratos AXIS-165) equipped with a monochromatic Al $K\alpha$ (1486.6 eV) x-ray source and
concentric hemi-spherical analyzer coupled with a charge neutralizer operated at 15 kV and 10 mA.

The ALD of hafnium oxide made use of tetrakis (diethylamino) hafnium (TDEAH) with water vapor as the oxidizer within a hot wall ALD reactor maintained at 200 °C. Further details of the ALD reactor can be found elsewhere [40, 87]. In these studies, 0 – 50 ALD cycles were used on the copper patterned silicon substrates in order to probe and evaluate selectivity of ALD on both silicon and copper surfaces simultaneously on the same substrate. The ALD kinetics of HfO₂ under these conditions on silicon has been previously examined [115] and under these typical reactor conditions, a self-limited ALD rate of 0.11 nm/cycle is observed with excellent linearity with respect to the number of applied ALD cycles, without an initial inhibition period.

4.4.3. Results and discussions

Figure 44 shows XPS survey scans of copper and silicon portions of the substrate after 0, 25 and 50 ALD cycles of HfO₂ on three copper patterned silicon substrates. The spectra labeled (a) through (c) represent survey scans on the silicon portion of the substrates, while spectra labeled (d) through (f) represent survey scans on the copper portion of the substrates. Prior to deposition, XPS analysis of the silicon surface indicates only Si, O and C elements (figure 44a). The carbon is the result of surface contamination [115] and the oxygen comes from the native oxide on the silicon surface. After 25 and 50 ALD cycles (figures 44b and 44c, respectively), several XPS peaks appeared on the silicon portion of the substrate which correspond to Hf 4f (15.5 - 20.3 eV), Hf 4d (213.7 - 225.8 eV), and Hf 4p (382.5 eV and 440.3 eV). The intensity of
these XPS peaks increases with increasing number of ALD cycles, while at the same
time, the Si 2p (98.0 eV) and 4s (150.1 eV) peak intensities decrease due to the growth
of HfO$_2$ on top of the silicon surface. The thicknesses of the resulting HfO$_2$ films on
silicon after 25 and 50 cycles are 2.8 nm and 5.4 nm, respectively, as measured by
ellipsometry and they are consistent with our previously evaluated HfO$_2$ ALD rate of
0.11 nm/cycle on patternless silicon substrates.
Figure 44. 0, 25, 50 ALD cycles of HfO₂ on Si (a, b, c) and Cu (d, e, f); (a) and (d) corresponds to 0 cycle, (b) and (e) to 25 cycles, and (c) and (f) to 50 cycles. ALD reaction temperature is 200 °C and the pressure is 0.18 Torr
On the copper portion of the substrate with no ALD cycles, the XPS survey scan shows Cu 2p (932.2 eV and 952.0 eV) which indicates that copper is mainly in the metallic state (figure 44d) \cite{116}. A small O 1s peak is also observed which is consistent with the trace presence of native copper oxide on the surface which was also detected by ellipsometry. After 25 ALD cycles of HfO$_2$, the XPS analysis still shows no hafnium-containing species on the copper portion of the substrate (figure 44e). Compared to Hf 4f peak of HfO$_2$ on silicon at 25 cycles, this result represents at least a 60-fold reduction of Hf on the copper surface at 25 cycles indicating less than one monolayer of Hf one the copper surface. The XPS peaks observed beyond 570 eV binding energies correspond to copper with trace amounts of surface oxide as noted on figure 44(d-f) with slight increase of oxides after ALD due to air oxidation of the copper upon removal from the heated reactor while still hot.

After a further increase of the HfO$_2$ ALD cycles to 50 (figure 44f), Hf 4f and Hf 4d peaks become detectable indicating eventual HfO$_2$ growth on the copper surface. The significant time delay in the formation of HfO$_2$ on copper indicates the need for surface site nucleation of HfO$_2$ on copper which is not present on silicon. This is surprising since both copper and silicon have native oxides on the surface. It is noted that in figure 1f the intensity of the Cu 2p peaks decreased after 50 ALD cycles, further supporting the deposition on copper after that number of cycles.

Elemental compositions shown in Table III are calculated from quantitative analysis of the XPS spectra of the corresponding elements. The increased amounts of
hafnium and oxygen along with the decreased amounts of silicon from 0 to 50 ALD cycles indicate the continuous growth of HfO$_2$ films on the silicon portion of the substrates. On the other hand, HfO$_2$ deposition on the copper portion of surfaces is observed only when more than 25 ALD cycles of TDEAH/H$_2$O are used.
Table III. Elemental compositions (at. %) on Si and Cu parts of substrate surfaces determined by XPS after 0, 25 and 50 cycles of ALD hafnium oxide

<table>
<thead>
<tr>
<th>ALD cycles</th>
<th>On Silicon (elemental composition, at. %)</th>
<th>On Copper (elemental composition, at. %)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hf</td>
<td>Si</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>58</td>
</tr>
<tr>
<td>24</td>
<td>24</td>
<td>18</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>3</td>
</tr>
</tbody>
</table>
Figure 45 shows XPS core spectra of Hf 4f after 25 and 50 ALD cycles of HfO₂ on both silicon and copper portions of the substrate surface. All spectra except the 25 ALD cycles of hafnium oxide on copper show the typical Hf peaks at 17.0 eV, Hf 4f₇/₂, and at 18.6 eV, Hf 4f₅/₂. No shoulder peak at lower binding energy is observed indicating no formation of other hafnium species, such as hafnium silicide, during the deposition [⁶₀, ¹⁰²]. From the Hf 4f core data after 25 ALD cycles on silicon and copper portions, the selective growth of HfO₂ on silicon over copper, that is, without any HfO₂ growth on the copper surface, is again demonstrated and clearly evident; at the same time, 2.8 nm of HfO₂ forms on the silicon surface. When the number of the ALD cycles increased to 50, it is found that there is a small amount of HfO₂ on the copper surface of the substrate indicating considerable delay in the formation of HfO₂ on copper surfaces and a significantly smaller amount of HfO₂ formed on copper than that on silicon. The likely explanation of this selectivity of HfO₂ ALD on silicon over copper is a significantly longer nucleation time for the HfO₂ ALD on copper than that on silicon, as silicon oxide easily accommodates hydroxyl sites at the surface. As a result, a growth inhibition period of HfO₂ on the copper surface is observed at a number of ALD cycles greater than 25. Further studies are needed to examine in greater detail the factors leading to surface selectivity and potentially identify means of further extending the inhibited growth on metallic copper and other surfaces relevant to nanofabrication of patterned thin film deposition used today.
Figure 45. XPS core scans ALD of HfO$_2$ on silicon and copper surfaces of patterned substrates. Experimental conditions for these samples are the same as those in figure 44.
4.4.4. Summary

In conclusion, copper patterned silicon substrates with different number of ALD cycles of HfO$_2$ have been carried out with films characterized by spectroscopic ellipsometry and XPS. The growth rate on the silicon portion of the copper patterned silicon substrate is 0.11 nm/cycle, which is similar to that previously observed on patternless silicon. XPS spectra show highly selective ALD growth of HfO$_2$ on the silicon surface over copper surface up to at least 25 ALD cycles, and this permits HfO$_2$ selective growth up of ~3 nm on the silicon portion of substrate with less than one monolayer ALD HfO$_2$ layer on the copper portion of substrate. In the current trends of semiconductor manufacturing, ~3 nm HfO$_2$ is sufficient in, for example, copper diffusion barrier layer on inter-level dielectrics. Therefore, such selectivity of ALD on different surfaces without any special surface modification can be quite significant and can have major impact on the nanofabrication of semiconductor devices in the future.
4.5. **Investigation on the Initial Growth of Atomic Layer Deposited TiO\textsubscript{2} Films on Silicon and Copper Surfaces**

4.5.1. **Introduction**

TiO\textsubscript{2} thin film has attracted considerable attention due to its chemical stability, photocatalytic activity, high dielectric constant and so forth, which make it suitable for variety of applications [59, 117-119]. For example, the high refractive index with the excellent transmittance in the visible and near-IR spectral regions has led to its extensive application in antireflection coatings and pigments [120]; its photocatalytical activity has made this material of interest for application in photocatalysis, such as photodecomposition of water, photodegradation of acids and photot_reduction of carbon dioxide [121-123] most recently, it was reported that the dielectric constants of TiO\textsubscript{2} and Al-doped TiO\textsubscript{2} films were significantly enhanced by growing through atomic layer deposition on Ru electrodes, which is because of the structural compatibility between rutile TiO\textsubscript{2} and in situ formed RuO\textsubscript{2} at the interface [124], such finding has exposed the TiO\textsubscript{2} based composite films as promising gate oxide candidates in DRAM application.

Atomic layer deposition (ALD), is a method to grow thin films through self-limiting surface reactions between cyclic introduced gaseous reactants [125]. It is considered as one of the most promising deposition methods to form the conformal TiO\textsubscript{2} films on the flat surface of silicon as CMOS gate oxide, on the three dimensional hole structure in DRAM devices as well as on complex structures for nanomaterials. There are numerous reports concerning the deposition of TiO\textsubscript{2} thin films using ALD on the effects of applied precursors, oxidant and deposition conditions on the film properties [48, 52, 90, 126, 127]. In those studies, TiO\textsubscript{2} film growth behavior and reaction mechanism were elaborated,
however, there quite a few studies [128, 129] concerning the mechanistic details of the TiO$_2$ film nucleation and growth chemistry, especially for the initial growth stage. In Cho, et. al’s report, TiO$_2$ was deposited on Si (100) substrate using the ALD-like cyclic MOCVD (Metal Organic Chemical Vapor Deposition) method with Ti(O'Pr)$_2$ and O$_2$, two steps were observed for growing SiO$_x$ and SiTiO$_x$ before forming bulk TiO$_2$ films; in the report of Methaapanon, et. al, TiO$_2$ was grown on OH/H terminated silicon(100) substrates using ALD with TiCl$_4$ and H$_2$O, in that report, no film nucleation stage was found on both surfaces, but with Ti-O-Si formed as interfacial layer on OH-Si and with Ti-Si formed as interface on H-Si.

In the initial ALD growth stage, the nucleation of a deposited material is strongly dependent on the physical/chemical properties of the substrate surface, on which the ALD surface reaction occurs. Nucleation on the substrate surface may differ from the steady growth stage due to the different surface chemistry the film grows on. Film initial formation properties, such as, roughness, island formation, nucleation, interfacial bonding, would affect the quality as well as the film properties after grown in bulk, especially when the scale of required film is quite small, such as the copper barrier with thickness only about a few nanometers, it is thereby important to understand and control the initial deposition onto different types of substrate in order to meet the desired characteristics and stringent requirement for such thin films. To the authors’ best knowledge, the investigation of TiO$_2$ initial growth as well as bulk film properties on Cu substrate have not been explored.
In this report, atomic layer deposited TiO$_2$ films grown on Cu and Si substrate surfaces are investigated with focus on the comparison of the initial growth stages on both surfaces. The Cu surface is patterned on the Silicon substrate for assuring the comparison of film initial growth behavior are based on the 100% identical deposition conditions. This study is of great importance in the area of selective atomic layer deposition induced by different surface chemistry \cite{130,131} and application of TiO$_2$ as copper diffusion barrier (figure 46), which require only a few nanometer-thick layer grown on the silicon based Inter-Level Dielectric (ILD) with negligible growth on the copper based Via of microelectronics \cite{132}.
Figure 46. Scheme of copper diffusion barrier between Via and ILD.
4.5.2. **Experimentation**

In this study, about $2 \times 2$ cm$^2$ sections of silicon (100) substrates were firstly cleaned by RCA SC-1 (Radio Corporation of America Standard Cleaning) solution to remove organic contaminants followed by 1% HF dip for 10 s, the remaining native oxide is about 1 nm after this cleaning recipe. The cleaned silicon substrates were masked by another piece of silicon (one-half of the substrate) face-to-face followed by about 200 nm copper evaporation on masked substrates through electron beam evaporation (Varian model no. NRC3117). After copper was partially coated on silicon, the patterned substrates were exposed to clean room air for 24 hr, which generated about 1 nm native oxide on copper portion of substrate through natural oxidation while the oxidation on the silicon portion is negligible. Thicknesses of the native oxides on both surfaces were measured by a spectral ellipsometer (Woollam M-44). The purpose of designing such copper patterned substrate is to ensure both surfaces subjected to 100% identical deposition conditions with comparable amount of native oxide on both surface portions. To minimize any additional oxidation of the copper surface portion, the ALD of TiO$_2$ was done consecutively from 5 to 200 cycles using metal precursor tetrakis (diethylamino) titanium (TDEAT) and H$_2$O as oxidant. After ALD, film thickness were measured by spectral ellipsometry (Woollam M-44, equipped with a high voltage lamp power supply: LPS-400) and X-ray photoelectron spectroscopy (XPS, Kratos AXIS-165, equipped with a monochromatic Al $K\alpha$ (1486.6 eV) X-ray source and concentric hemispherical analyzer), which was also employed to probe the chemical bonding as well as elemental concentration for TiO$_2$ films grown on both surfaces from 5 to 70 cycles; surface morphology of the samples was probed by a noncontact interferometer precision surface profiler WYKO NT 3300 with working mode of Phase Shifting.
Interferometry (PSI). The PSI measurements allow obtaining a vertical resolution as high as 0.3 nm with 20x objective over a surface area of about 0.07 mm².

4.5.3. **Results and discussions**

Figure 47 shows the growth rates of TiO₂ on silicon surface portion and copper surface portion of substrates through ALD. The reaction temperature was 200 °C with 6 s precursor pulsing. Error bars represent the standard film thickness deviations of three different points all across each portion of the substrate. On the silicon portion of substrate (figure 47 a), from both the initial deposition cycles (inset graph) and the large number deposition cycles (50 - 200), film thicknesses are observed with linear increment with growing number of deposition cycles, indicating the ALD-like growth kinetics. The calculated growth rate of TiO₂ on silicon surface portion is about 0.10 nm/cycle. Comparatively, the growth of TiO₂ on the copper portion of substrate only exhibit linear function with growing number of deposition cycles (more than 50 cycles), the calculated growth thickness from the slope is about 0.09 nm/cycle; as for the initial growth from 5 to 30 deposition cycles indicated in inserted figure 47 (b), at 15 and 20 cycles, the grown film thicknesses on copper portion surface are the same about 0.2 nm, such steady region was also found by Cho, et al [128] and Methaapanon et al [129], which was observed as the incubation period before bulk film growth. The bulk film starts to form on copper portion surface only after 25 cycles with film thicknesses larger than 0.5 nm. This indicates growth of TiO₂ on copper surface portion undergoes a considerable delay of film formation (25 cycles or more) compared with film growth on silicon surface (less than 5 cycles nucleation period).
Figure 47. Measured film thicknesses on silicon and copper of substrates.

Depositions were carried out at 200 °C with 6s precursor pulsing and 50 ms for H₂O pulsing. The base pressure of reactor was 0.2 torr.
Figure 48 shows the corresponding XPS core scans of the Ti 2p on copper and silicon portion of substrates subjected to 5 to 30 ALD cycles of TiO$_2$. On silicon surface portion, as figure 48 (a) shown, all Ti 2p spectra exhibit Ti 2p$_{5/2}$ and Ti 2p$_{3/2}$ peaks with the standard line separation of 5.7 eV on silicon associating with the formation of Ti$^{4+}$. There lacks any shoulder peak formation at the lower binding energy of Ti 2p peaks suggesting the good interface between TiO$_2$ films and the underneath SiO$_x$/Si substrate without formation of TiSi$_x$ species [103, 104]. Correspondingly, the Ti 2p spectra on the on the copper portion surfaces exhibit very noisy and much weaker signals compared with those on silicon portion surfaces. Deviation of peak position of Ti 2p$_{3/2}$ is also observed and could be explained by the considerable film incubation cycles with respect to negligible (or less than five cycles) incubation cycles on silicon portion of substrates. Much smaller XPS intensity of Ti 2p peaks on copper surface portion was observed, indicating the island-like type of growth behavior of TiO$_2$ film at its initial grow stage—island-like nucleation would leave relatively large uncovered substrate surface area by Ti nuclei, which results in lower XP spectra intensity [133]. This result is also supported by the surface morphology & roughness of TiO$_2$ on copper portion of substrates in the later discussion.
Figure 48. XP spectra of the Ti 2p core scans on silicon portion (a) and copper portion (b) of substrates from 5 to 30 cycles.
Changes in the amounts of Si/Cu, O, and Ti with the number of deposition cycles are demonstrated in figure 49. Elemental compositions were calculated from quantitative analysis of the XP spectra of corresponding elements from 5 to 70 cycles’ depositions. Higher percentage of element corresponds to the increment of certain atomic species within the X-ray penetration of surface films. As figure 49 (a) shown, for the film grown on silicon portion of substrate, the silicon species decreases compared with increasing Ti and O species with growing cycle number from 5 to 70—indicating steady film growth on silicon portion. For the film grown on copper portion of substrate, with cycle number of 10 or smaller, the concentrations of Cu and O stay the same with no detected Ti species formation; at 15 cycles, Ti concentration was found to increase to 1.9% with no further increment of O observed, indicating the newly found Ti species could be in the form of Ti-O-Si (since no TiSi\(_x\) was found as previous discussion indicates) rather than Ti-O-Ti, suggesting TiO\(_2\) nucleation period is about 15 to 20 cycles. When cycle number further increases to 25 cycles or more, both Ti and O species percentages are seen to grow steadily, indicating formation of Ti-O-Ti bonding with cycle number at 25 or higher. The atomic ratio of Ti and O is higher than 0.5, for films grown on both portions of substrate, which is attributed to existence of native oxide at the interface.
Figure 49. Changes of atomic percentages as a function of deposition cycles (from 5 to 70) on silicon portion a (above) and copper portion b (down) of substrates.
Surface morphology and spike height distribution for 0, 15 and 30 cycles deposition on the patterned substrates were probed by surface profiler, as illustrated in figure 50 (on silicon surface portion) and figure 51 (on copper surface portion). The corresponding roughness parameters are presented in Table IV. Ra is the most common parameter used to calibrate surface roughness and Rq, which is also known as RMS (root mean square) roughness, provide the overall roughness heterogeneity across the surface—a small difference between the Ra and Rq indicates a low spike density and thereby a smooth surface. Rt stands for the distance between the highest peak and the lowest valley and provides information about spike height, but different from the statistical values of Ra and Rq, Rt only represents value of a single point. As can be seen from the 3D surfaces profiles of figure 50 (a) ~ (c), the undeposited silicon surface profile represents the morphology of SiOₓ native oxide formed on silicon surface; after 15 and 30 cycles deposition, a uniform coating with smaller RMS values was observed as an indication of TiO₂ film formation. Comparatively, the undeposited copper surface portion, as figure 51 (a) shown, exhibits a uneven morphology with slightly higher RMS roughness than that of silicon surface; after 15 cycles deposition, the surface became even rougher with visible island-like clusters (as highlighted in squares) indicating film underwent nucleation, leading to increased vertical spike density; after 30 cycles, the surface presented a much smoother morphology with comparable RMS roughness value to that on the silicon portion of substrate with the same number of deposition cycles.
Table IV: Measured values of surface roughness of 0, 15 and 30 ALD cycles of TiO$_2$ on silicon and copper substrates; the values of Ra (arithmetic average roughness), Rq (root mean square roughness) and Rt (peak to valley) are expressed in nm; the thickness of each sample are indicated in figure 47.

<table>
<thead>
<tr>
<th>ALD cycles</th>
<th>On Silicon (nm)</th>
<th>On Copper (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Ra</td>
<td>Rq</td>
</tr>
<tr>
<td>0</td>
<td>0.40</td>
<td>0.51</td>
</tr>
<tr>
<td>15</td>
<td>0.27</td>
<td>0.39</td>
</tr>
<tr>
<td>30</td>
<td>0.39</td>
<td>0.46</td>
</tr>
</tbody>
</table>
Figure 50. Surface morphology of TiO$_2$ on silicon surface portion with different ALD cycles at (a) 0; (b) 15; (c) 30.
Figure 51. Surface morphology and of TiO$_2$ on copper surface portion with different ALD cycles at (a) 0; (b) 15; (c) 30.
For a further understanding of film surface morphology, the RMS roughness of TiO$_2$ on silicon and copper portions of substrate were examine at different deposition cycles. As shown in figure 52, three regions have been identified as: a-no film formation, b-film nucleation and c-bulk film formation. Interestingly, the RMS roughness of silicon portion of substrate was reduced by 5 cycles deposition of TiO$_2$ (about 0.6 nm). This suggests TiO$_2$ film was grown on silicon substrate without a delayed in film nucleation, such phenomenon was also observed by Kim et al [133], who found the Au substrate surface roughness is reduced by growing 1 nm Ru film by ALD and it is most likely because that the ALD resulted films posses much smoother surface than the native oxide films formed on the surface. From 5 to 100 cycles deposition of TiO$_2$ on silicon surface portion, RMS roughness slightly increases with growing cycle number indicating the full area film coverage starts from 5 cycles. On the copper portions of substrate, little change of RMS surface roughness was found from 0 to 10 cycles as a sign of no change of surface morphology, because no film formed during that region; the peaks of RMS values were found at 15 and 20 cycles, further confirming the TiO$_2$ film nucleation period from 15 to 20 cycles with maximized vertical densities; with cycle number increased up to 30 or more, the RMS values decreased to a comparable level as that on silicon portion of surface, the resulting smoother surface is associated as continuous bulk film formation of TiO$_2$, also, the trend of slightly increased RMS value with growing cycle number on copper surface is very similar to that on silicon surface portion.
Figure 52. RMS surface roughness distributions as a function of deposition cycle number on both silicon and copper surface portions.
4.5.4. Summary

The initial growth of atomic layer deposited TiO$_2$ on silicon and copper surface was investigated by Ellipsometry, XPS and surface profiler. TiO$_2$ thin films were grown on copper patterned silicon substrate using TDEA-Ti precursor and H$_2$O as oxidant. The TiO$_2$ growth rate on silicon portion of substrate is 0.10 nm/cycle, which is slightly higher than that on copper portion of substrate (0.09 nm/cycle). On silicon surface portion, it exhibits a linear growth rate for TiO$_2$ from 5 to 200 cycles with negligible (or less than 5 cycles) incubation period; on copper surface portion, however, the initial growth of TiO$_2$ is not ideally linear with considerable delay of film formation due to initial nucleation. Both XPS and surface profiler results show the island-like growth during film nucleation resulting in very rough surface morphology on copper at 15 and 20 deposition cycles. In addition, XPS results indicate the formation of the structure of Ti-O-Si in stead of Ti-O-Ti during film nucleation on copper surface portion. Although TiO$_2$ films were deposited on the both OH terminated surfaces with comparable amount of native oxide, the initial growth mechanisms on different substrate chemistries differ greatly; further studies will be needed to bring more detailed insights into how the difference chemistries of substrates would affect film nucleation mechanism. This study is rather important in the areas such as Selective ALD applications and growth of copper barrier by ALD.
4.6. Atomic Layer Deposition of HfO$_2$ on Silicon and (PMMA) Polymer Fibers

4.6.1. Introduction

Material science for the improvement of humanity's needs and desires has driven extensive research into novel materials for many diverse applications. Building micro and nanoscale devices has created great demand and interest for the most elective and suitable materials at unprecedented reduction in size. As the electronic circuitry continues to decrease, atomic layer deposition (ALD) has become more widely utilized as it allows for excellent control of film thickness and composition down to the atomic scale.

One important application of ALD has been the fabrication of modern electronic devices. Over recent years, the demand for higher density integrated electronics has increased and, to maintain cost competitiveness, the dimension of transistor size has decreased roughly by a factor of 2 every two years. To maintain this aggressive pace, the semiconductor industry identified the need for new materials with higher dielectric constants than silicon dioxide to be integrated into their fabrication processes. Research on many different metallic oxides has led to the identification of hafnium oxide and other transition metal oxides as the promising high dielectric materials for future electronic devices. In fact, Intel recently announced production plans for their new microprocessor involving hafnium containing films [15]. In recent years, new nanostructure materials have been explored for numerous applications. For example, carbon nanotubes (CNTs) have proved to be an extremely good material for enhancing material tensile properties [134]. The search for novel dielectric materials in transistors provided the impulse for research concerning inorganic nanotubes to complement the CNT research. In other
applications, inorganic nanotubes hold promise for energy storage and hydrogen sensing [135].

Various inorganic materials have been transformed into nanotube structures. Two inorganic materials with tremendous technological impact are titania and alumina. Titania, which also possesses a high dielectric constant, has been very popular for inorganic tube formation [41]. Titania and alumina nanotubes have actually been constructed through ALD over polymer fibers serving as a template for nanometer scale shapes [121]. The polymer fibers are then vaporized at higher temperatures to leave behind the metal oxide nanotubes. In an alternate approach, other research groups have coated CNTs in various inorganic materials, including HfO₂ [136]. To the authors' knowledge, inorganic nanotubes have not been constructed from a deposition of hafnium oxide on polymers. Such nanotubes may have applications in several nanofluidics and electrical engineering systems.

ALD has allowed for carefully guided control over the thickness growth of a thin film. In this technique, one or more gaseous precursors can be reacted with an oxidizer upon a substrate under a vacuum to construct each row of atoms of a thin film. The thickness of the film from such a method has been correlated to the number of deposition cycles, wherein a cycle involved precursor exposure, nitrogen purging, an oxidizer pulse, and subsequent purging. In constructing nanotubes, ALD provides controlled deposition with high surface conformity over fibers. In this study, the gaseous precursor tetrakis (diethylamino) hafnium (TDEAH) with water being the oxidizer has been used for the
deposition of hafnium oxide over poly-caprolactone (PCL) fibers with the ultimate goal of fabricating hafnium oxide nanotubes.

4.6.2. **Experimentation**

In the deposition of hafnium oxide on silicon, Boron P-doped silicon (100) wafers are cut into smaller –15 x 17 mm pieces from their original 100 mm diameter wafer by a diamond cutter. De-ionized water from a Barnstead Nanopure Infinity ultra pure water system was used for the cleaning of the small silicon samples. After being dried with nitrogen gas, the silicon substrate was loaded into a notched quartz holder. Alternatively, for deposition onto fibers, electrospun poly-caprolactone (PCL) fibers with diameters – 0.5 - 1 um were spread across an approximately 4 x 7 mm window in aluminum foil. The foil holding the fibers was placed inside a stainless steel envelope with 3 £ 9 mm windows on both sides of the envelop. The envelope provided support when inserted into the notched quartz holder. The substrate was placed 35 cm down a quartz tube inside the reactor, which has been described elsewhere [49], before the vacuum pump returned the chamber to 0.170 torr. The hafnium precursor was tetrakis (diethylamino) hafnium (TDEAH), being heated to 67 °C in its bubbler. Precursor gas flowed from its bubbler through a gas port connection region at 75 °C and a manifold junction maintained at 160 °C prior to entering the reactor. The LabView computer program-interface system controlled purge time and precursor pulses electronically. Three to five precursor pulses per ALD cycle were used to inject the precursor into the reactor during 50 cycles. The purge time between cycles consisted of 20 seconds, compared to 10 seconds between precursor and oxidizer. The oxidizer gas was water vapor carried by a N₂ gas stream that passed through a water bubbler maintained at 0 °C using an ice bath. During the
deposition on polymer fibers, the reactor pressure must be pumped up and down gradually in order to not blow away the fibers from the abrupt pressure gradient. The PCL fibers were formed by electrospinning the polymer from beads (CAS 24980-41-4). And since PCL melts at about 60 °C, the reactor was maintained below this temperature to prevent melting of the fibers.

The spectral ellipsometer was used to determine the thickness of films from an optical model for hafnium oxide on silicon with 15 Å of native oxide present. The J. A. Woollam Co., Inc., Model M-44 ellipsometer was calibrated daily with a silicon dioxide standard. The substrates for each trial were annotated and stored in plastic Petri dishes. X-ray photoelectron spectroscopy (XPS) was conducted on a Kratos AXIS-165 Surface Analysis System with a 1486.6 eV Al K® source. XPS measurements were carried out at high vacuum (about 10⁻⁸ Torr). All scans were executed before and after Argon ion sputtering for removing surface contamination. A Hitachi S-3000 N scanning electron microscope (SEM) was employed for high magnification pictures of the resulting fibers. The aluminum portions of the packets were attached to the examination slide, leaving the electrospun fibers without contact with the carbon spots on the slide.
Figure 53. Average film thickness of HfO$_2$ on silicon at 5 TDEAH pulses per cycle for 50 cycles at various reactor temperatures.
4.6.3. **Results and discussions**

In previous studies, the ALD range for the hafnium TDEAH precursor has been shown at 200-275 °C \[^{[50]}\]. In this work at much lower temperature, a growth rate has been difficult to pin down - ranging from sub-angstrom to over three angstroms per cycle. The variation in growth rate maybe, in part, due to deposition chemistry outside the ALD range. The thickness has varied between runs under the same conditions of precursor pulses per cycle and reactor temperatures. Variation over reactor temperature at five pulse precursor dosage per cycle has shown no visible trend in growth thickness, as seen in figure 53. Thicknesses indicated here result from 50 total cycles and thus indicate a growth rate per cycle about two times higher than that for measured at higher temperatures with the same reactor \[^{[19]}\]. The film thickness on the substrate is less where the notch covered the substrate. At the very top of the substrate, discoloration has occurred to a burnt-brown color from the increase in hafnia present along this edge. Beyond the discoloration for the extreme edge increase, the silicon substrates display thickness variations up to 25%. Given the observed growth rate and nonuniformity, the ALD process has likely been compromised by going to such a low temperature. However, for this application, these deposition characteristics may be sufficient.

XPS has long been employed to investigate the identity of thin film materials. The possibility of carbon contamination at low temperatures is typically a concern, when using an organometallic precursor. XPS investigation of hafnia deposition on silicon at 30-80 °C revealed significant carbon presence in the samples. At these low temperatures, the atomic carbon presence has ranged between 7-13\% after Ar\(^+\) sputtering or the surface.
As seen in Figure 2, the hafnium 4f doublet at 17.6 eV and 19.3 eV is indicative of Hf-O bonding for aforementioned samples. However, the hafnium 4f doublet in Figure 2 for the 70 °C and 80 °C runs bulged out into an attached peak around 15.8 eV, suggesting the presence of Hf-N bonds [137]. Running the reactor consistently every day has probably prevented problems, such as the extra Hf-N bonds from having a significant presence in XPS samples. Therefore, at this time, the presence of Hf-N is suspected to be from reactor contaminants and not a temperature effect. Typically with this reactor, the first runs each day were purging runs to prepare the system for clean deposition.

After the promising runs with low temperature growth of hafnium oxide films on silicon, the direction turned to deposition on PCL fibers held in aluminum foil packets. Various challenges arose in preserving the fragile fibers. The reactor pressure must be slowly changed in order to retain the fibers intact in their packets. In order to maintain a low temperature, the heat strip and thermocouple must remain connected because disconnecting and reconnecting the thermocouple induced a temperature spike above the melting point. The gas pulses were delivered through a feed tube, which could blow away fibers that were too close. However, fibers those were too far away did not receive deposition coverage. Mechanical support for the PCL fibers was also a concern for the foil falling over. A silicon substrate was initially used to support the foil, but the fibers could break upon contact with the substrate.
Figure 54. XPS Hf\textsubscript{4f} of HfO\textsubscript{2} deposited on Si at various temperatures. The doublet seems to acquire a bulge at 15.8 eV at 80 °C of an Hf-N bond, suggesting an incomplete reaction with the precursor. Lower temperatures reveal no such bonding. Intensities have been vertically shifted for visibility and are not meant to be considered on a common intensity scale.
A stainless steel envelope was designed specifically to fit inside the reactor tube and quartz boat notches. Separation between the metal sides was just wide enough to figure. 55: Scanning Electron Microscope image of hafnia-coated PCL fibers suspended between aluminum foil under 25 x magnifications. Deposition occurred for 100 cycles on each side at conditions of 30 °C and 0.170 torr contain the foil packet holding the PCL fibers, with a window appropriately sized over the fiber location. Gas would now either deposit on the fibers or pass through the setup. Movement of the foil or fibers from pulsing was greatly reduced. If the envelope moved, everything would move together - the fibers could no longer knock into anything to break. Operating at 30 °C and 0.170 torr standby pressure, the reactor setup delivered 100 deposition cycles with 4 precursor pulses per cycle to deposit hafnium oxide on each side of the fibers. Due to the large density of fibers supplied in each foil packet, visual presence confirmed the survival of the fibers, as shown in Figure 55 under 25 x magnifications. In observing fibers under the electron microscope, fibers' diameter ranged in size between 0.5-1.0 microns. Under 1000x magnification for back-scattering, the hafnium oxide coverage could be seen over many of the fibers shown in Figure 56.
Figure 55. SEM image of hafnia-coated PCL fibers suspended between aluminum foil under 25x magnification. Deposition occurred for 100 cycles on each side at conditions of 30 °C and 0.170 torr.
Figure 56. SEM image of hafnia coated PCL fibers under 1000x magnification.

Other conditions are the same as in Figure 55.
In back-scattering, elements with higher atomic numbers appear lighter; consequently, at an atomic number of 72, hafnium has a bright white appearance over the darker, lower-numbered carbon. The energy dispersive X-ray (EDX) scan of the white coating confirmed the significant presence of hafnium and oxygen along with the carbon-based polymer. As shown in figure 57 and figure 58, the fibers show near-continuous coverage by hafnium oxide.
Figure 57. SEM image of hafnium oxide deposited on PCL fibers with high coverage at 10000x magnification. Other conditions are the same as in Figure 55.
Figure 58. Close-up SEM image of hafnium oxide deposited on PCL fibers with high coverage at 4000x magnification. Other conditions are the same as in Figure 55.
4.6.4. **Conclusion**

Tetrakis (diethylamino) hafnium and water can be employed in the deposition of hafnium oxide films all the way down to room temperature at 30 °C. At the lower temperatures, such films show relatively high non-uniformity with variations up to 25% in thickness. With proper orientation, hafnium oxide will deposit over PCL fibers. For a sufficient number of cycles, the fibers would be coated completely in hafnium oxide; the expectation is that 150 cycles would be the minimum number of cycles for complete coverage. After deposition, vaporization of the polymer would then leave the desired hafnium oxide nanotubes. With the fibers supported in the stainless steel envelope frame, the number of cycles could be increased without concern for breakage from the additional pulsing. Proof of concept for the creation of hafnium oxide nanotubes has shown promise through the preliminary findings of this work. Future work could be to increase number of cycles for better coverage and vaporize the PCL to create the freestanding nanotubes. After fabrication, the nanotubes could then be tested for electrical, chemical, and mechanical properties to determine their potential in future applications.
4.7. **Atomic Layer Deposition of Al₂O₃ on Si (100) as Buffer Layer for HfₓTi₁₋ₓO₂**

4.7.1. **Introduction**

Gordon E. Moore stated that the number of transistors on an integrated circuit doubles every two years [5]. As simple as it may sound, this statement is the foundation of the semiconductor industry and its driving force for making smaller and faster transistors. The question that arises is an obvious one, how long can this scaling continue? So far, SiO₂ (dielectric constant (κ) = 3.9) has been the choice for the gate dielectric in transistors, but as Moore’s Law extends, the thickness of the SiO₂ layer would have to be continually reduced. Eventually, it would become just a few atomic layers thick (~1 nm). When the thickness of SiO₂ dielectric in transistors reaches this fundamental limit, electrical current would pass through it causing power losses and unwanted heat. Therefore, a new generation of higher dielectric constant materials is needed for the replacement of SiO₂ as gate dielectric layers. The leakage current can then be reduced by increasing the thickness of gate dielectric layer. Currently, our research group at the University of Illinois at Chicago (UIC) is developing new high κ dielectric materials which can be used in complimentary metal oxide semiconductor (CMOS) transistors and dynamic random access memory (DRAM) capacitors. There are many high κ materials that have dielectric constant higher than SiO₂ but not many are compatible with the Si substrate that is used in the semiconductor devices. Important concerns include interface quality, film morphology, and reliability [5]. I have previously determined the optimal conditions in which to produce high κ dielectric films of HfO₂ and TiO₂.

Hafnia has a κ value of 25 [59] and titania has a reported κ value above 30. Hafnia by itself is chemically stable with silicon but its κ value is moderate. Moreover, it
crystallizes at annealing temperatures higher than 600 °C. Doping it with titanium could possibly increase the overall dielectric constant value. Crystalline films crack upon annealing and it is thought that current leakage occurs at these boundaries [138]. Combining these two high κ materials could possibly increase the overall κ value to above 25 and yet maintain the beneficial amorphous structure. This would, therefore, allow for thicker gate dielectric layer in the transistor, and further minimize the tunneling effect and lower the leakage current. However, there are other related concerns such as how the combination of TiO₂ and HfO₂ would affect the conductivity of the film and the nature of the resulting interfacial structure at the high κ /Si interface. Studies have shown that the addition of an Al₂O₃ buffer layer between HfO₂ and the silicon substrate could prevent the formation of silicates and silicides during annealing [102]. The goal of this study is to grow a buffer layer of Al₂O₃ on silicon substrate before depositing nano-laminated composite structure of HfₓTi₁₋ₓO₂. The conditions to deposit the hafnia and titania films individually using the two precursors TDEAH and TDEAT, respectively have been established and a common ALD growth window has been observed that could be utilized for growing the composite HfₓTi₁₋ₓO₂ films. In order to grow the Al₂O₃ buffer layer in-situ, the existing ALD system needed to be modified to accommodate the third precursor (TDEAA). After the modification, the process parameters for ALD of Al₂O₃ using TDEAA need to be optimized. The final step would be to investigate the nano-laminated HfₓTi₁₋ₓO₂ films deposited on the Al₂O₃ buffer layer by varying the ALD cycle ratio of HfO₂ (using TDEAH) and and TiO₂ (using TDEAT).
In the first step of this study, the ALD reactor was reconfigured with the addition of the new TDEAA precursor as shown in Figure 59. Al₂O₃ was then deposited on Si(100) substrates by atomic layer deposition. In this process, the reactants are introduced in the reaction chamber in an alternating sequence involving pulses where each reactant pulse is separated by a purge step to remove excess reactant and reaction by-products. For depositing Al₂O₃ by ALD in our study, water vapor was used as the oxidizer (second reactant). This process is “self limiting” [139]. This is slightly different from chemical vapor deposition (CVD) in terms of the precise control of grown film thickness—during each repeated cycle only one saturated atomic layer will be formed. The procedure follows four basic steps: First, exposure of the substrate to the first precursor; the second step is a nitrogen gas purge to clear out the left over precursor, followed by the introduction of an oxidizer to produce the desired compound on the surface of the substrate; finally a nitrogen gas purge will clear out the system of any leftover gaseous reaction material [6]. The growth rate of Al₂O₃ was measured as a function of reactor temperature, precursor dosage (plugs), and number of deposition cycles.

One of the critical parameters for ALD is the ALD temperature window as shown in Figure 60. The deposition process carried out in this temperature window results in the self limiting reaction which is the characteristic of ALD [140]. The advantages of ALD include submonolayer thickness control, excellent uniformity and excellent step coverage. One of the limitations is that the deposition rates are relatively slower compared to other deposition methods [140].
4.7.2. **Experimentation**

The existing ALD system was modified to accommodate the third precursor TDEAA (referred to as C) in Figure 59 [49]. After the new valves and elbows were attached, care had to be taken to rewrap the valves and legs of the precursors with heat tape and insulating fabric to control heat loss in the delivery lines. Thermocouples were also attached to the new precursor and leg to provide feedback to the temperature controllers regulating the heating. After this was completed the optimization of ALD conditions for Al₂O₃ growth using TDEAA was carried out.

The ALD of TDEAA was performed in a hot wall tubular reactor using water as the oxidizer (Figure 59). As shown in Fig. 59, the manifold has two separate lines for moisture and precursor leading to the reactor. The details of the reactor setup are reported elsewhere [49]. Prior to deposition, 2 cm x 2 cm silicon squares were cut, thoroughly rinsed with deionized water, and dried with N₂ before loading to the ALD chamber. Adding a new precursor bubbler calls for re-tuning of the ALD setup since the addition of a new branch will break the formerly established optimization conditions; a series of parameters need to be found out before reaching the really ALD reaction conditions. The parameters include, precursor temperature, ALD temperature window, and the number of precursor pulses needed to saturate silicon surface. Immediately after deposition, the film thicknesses were measured using a spectral ellipsometer (J. A. Woollam Co., Inc., model M-44).
Figure 59. The schematics of the ALD system and the modification that was done to add precursor C (TDEAA).
Figure 60. Different reactions occurring in an ALD process. Acceptable window refers to the reactor temperature window in which the ALD growth occurs.
4.7.3. **Results and discussions**

Figure 61 shows the results from the initial steps that were taken to identify the optimal precursor (TDEAA) temperature so as to provide sufficient vapor for ALD reaction. A reactor temperature of 200 °C was used and 50 ALD cycles with and 5 precursor plugs were used since originally these were the conditions used for depositing films from the other precursor, TDEAH. The vapor pressure of TDEAA is 0.2 Torr at 100 °C as seen in figure 62 and the operating pressure range of our reactor is 0.2-1.5 Torr. From this information, it was decided to use a precursor (TDEAA) temperature of 85 °C as the starting point and increase it in increments of 5 °C until film growth was observed. An increase in film thickness from 0 Å to 60 Å was observed as the precursor temperature was increased from 85 °C to 105 °C. From these results, it was decided to keep the bubbler temperature at 100 °C for the remainder of the study since this temperature appeared to be enough to generate sufficient precursor vapor.
Figure 61. Al$_2$O$_3$ film thickness vs. the precursor (TDEAA) temperature for obtaining optimal precursor temperature.
Figure 63 shows the next steps taken to identify the optimal ALD conditions for ALD of Al₂O₃ from TDEAA. In these sets of experiments, the objective was to observe the self limiting reaction that is the characteristic of any ALD process. The temperature of the precursor was set at 100 °C based on the results from the earlier optimization step. The reactor temperature was set at 225 °C. The number of deposition cycles was 50. As the number of plugs of precursor pulse increased from 3 to 7, a linear increase of film growth rate was observed. For a number of plugs greater than 7, the growth rate stopped increasing and this indicates that a self limiting ALD reaction has been attained for 7 plugs of precursor pulse. Thus, seven plugs are found to be optimal for ALD of Al₂O₃ using TDEAA.
Figure 62. TDEAA vapor pressure vs. temperature
Figure 63 shows the results from the steps that were taken to identify the ALD temperature window for growth of Al₂O₃ using TDEAA. The reactor temperature was varied while the optimal parameters found in the previous steps were used for the ALD process. The growth rate is between 1.5 and 2.0 Å/cycle at a reactor temperature of 150 °C which could be the result of condensation of the precursor. The growth rates become constant (1-1.5 Å/cycle) between 200 °C and 275 °C indicating an ALD growth window ranging from 200 °C to 275 °C. For reactor temperature higher than 275 °C, the growth rate increases dramatically probably due to the decomposition of the precursor.
Figure 63. Al$_2$O$_3$ film thickness vs. number of precursor plugs. Film growth saturation occurs at 7 plugs.
Figure 63 shows the film thickness versus the number of ALD cycles for the films deposited at the optimal ALD parameters. It can be observed that with the increase the number of deposition cycles from 25 to 125 a linear increase in the film thicknesses occurs. The average growth rate as calculated from the slope is 1 Å/cycle. This is indicative of monolayer growth control.
Figure 64. Al₂O₃ growth rate vs. reactor temperature. Self-limiting growth occurs between 200 °C and 275 °C.
Figure 65. Al$_2$O$_3$ film thickness vs. number of ALD cycles. An ALD growth rate of 1 Å/cycle is achieved.
4.7.4. **Summary**

The existing ALD system was reconfigured to add a third precursor (TDEAA). The optimal conditions for atomic layer deposition of Al$_2$O$_3$ were obtained. The optimal precursor (TDEAA) temperature was found to be 100 °C. The minimum number of plugs for a self limiting reaction was found to be 7. The ALD temperature window was found to be between 200 °C and 275 °C. At these optimal parameters, a film growth of 1 Å/cycle was obtained for ALD of Al$_2$O$_3$ films.
5. CONCLUSION

5.1. **Enhanced dielectric properties of Y doped HfO₂ by structure transformation**

Sequential Atomic Layer Deposition was used to deposit yttrium-doped hafnium oxide films with variable yttrium content using tris(ethylcyclopentadienyl) yttrium, and tetrakis(diethylamino) hafnium as metal precursors and water vapor as the oxidizer. The structure and electrical properties of the resulting films were analyzed after different post-deposition annealing conditions to assess composition-structure-dielectric property relationships. 2.5–100% yttrium-doped films annealed above 600ºC for 5 minutes consistently yielded cubic-HfO₂ structures. However, there was a strong compositional effect on the dielectric constant, which maximized at ~14% yttrium content. The films studied had leakage current density of 10⁻⁵ A/cm² or less at 1 V.

5.2. **Ar⁺ surface sputtering impacts on HfO₂ and TiO₂ films as well as optimization of ALD on film quality**

Tetrakis (diethylamino) hafnium (TDEAH) and tetrakis (diethylamino) titanium (TDEAT) were used for the atomic layer deposition (ALD) of HfO₂ and TiO₂ films on silicon (100) substrates with water being the oxidant. Studies on the decomposition temperatures of both metal precursors within the reactor itself and on the reaction temperature dependence of film growth rates and carbon impurity helped determine the optimal atomic layer deposition temperature range. X-ray photoelectron spectroscopy showed that after a short Ar⁺ sputtering to remove surface contaminants, both HfO₂ and TiO₂ were found to be carbon-free when films were deposited within the optimal ALD temperature window. However, Ar⁺ sputtering of the surface altered the chemical state of
and led to the formation of lower oxidation states of titanium. Optical profiling in the phase-shifting interferometry mode and grazing incidence X-ray diffraction were applied to probe the change of surface morphology and film crystallinity upon post-deposition annealing at 600 °C for 5 minutes. Capacitance-voltage (C-V) and current-voltage (I-V) measurements were performed over a metal-insulator-semiconductor structure after electron beam evaporation of 150 nm-thick Al metal contacts on the dielectric layers; the calculated dielectric constant, $k$, of TiO$_2$ was found to be about three times higher than that of HfO$_2$ and the measured leakage current densities for both metal oxides were below $2 \times 10^{-5} \text{ A/cm}^2$ at 1 V.

5.3. **Stabilization of amorphous structure of HTO upon 1000 °C annealing**

Tetrakis (diethylamino) hafnium (TDEAH), tetrakis (diethylamino) titanium (TDEAT) and H$_2$O were used for the atomic layer deposition of HfO$_2$, TiO$_2$ and Hf$_x$Ti$_{1-x}$O$_2$ films on silicon substrates. The atomic layer deposition (ALD) temperature windows were found to be 175 - 250 °C for HfO$_2$ (0.12 nm/cycle) and 150 - 250 °C for TiO$_2$ (~0.06 nm/cycle). The 175 - 250 °C overlap region is ideal for ALD of Hf$_x$Ti$_{1-x}$O$_2$ films. Different compositions of Hf$_x$Ti$_{1-x}$O$_2$ were obtained by varying the [TDEAH/H$_2$O]:[TDEAT/H$_2$O] cycle ratios and excellent tunability of film composition was found using X-ray photoelectron spectroscopy (XPS). The Hf$_x$Ti$_{1-x}$O$_2$ deposition rate was found to be superposition of the two individual growth rates. Both as-deposited to post-deposition annealed films were studied with XPS, phase shift interferometry, and grazing incidence X-ray diffraction. As-deposited HfO$_2$ and TiO$_2$ films were found to be amorphous and they began to crystallize after annealing at 600 °C in the monoclinic
phase (HfO$_2$) and in weak anatase phase (TiO$_2$). The Hf$_x$Ti$_{1-x}$O$_2$ films remained amorphous after annealing up to about 1000 °C in N$_2$ for 5 min.

5.4. **Selective Atomic Layer Deposition on copper patterned silicon led by different surface chemistry**

Selective Atomic Layer Deposition (ALD) was performed on copper patterned silicon substrates to selectively deposit HfO$_2$ film on silicon. The selectivity is based on differences of surface physics/chemistry rather than use of any molecular masking such as self-assembled monolayers. On silicon, the growth rate of HfO$_2$ is 0.11 nm /cycle with no initial inhibition of film growth, while on copper no HfO$_2$ deposition was observed up to at least 25 ALD cycles. The selective growth on silicon over copper at 25 ALD cycles provides a patterned film deposition at thicknesses of 2.8 nm HfO$_2$ which is relevant to semiconductor nanofabrication.

5.5. **Initial nucleation of TiO$_2$ on copper and silicon**

Atomic layer deposition (ALD) of TiO$_2$ using Tetrakis (Diethylamino)-Ti (TDEAT) precursor and H$_2$O was studied on silicon and copper surfaces—these two surfaces were patterned on the same substrate in order to insure the identical deposition conditions with comparison of the initial growth of TiO$_2$ on both surfaces. Ellipsometry, X-ray photoelectron spectroscopy and surface profiler were employed to probe the film growth rates, nucleation mechanisms as well as surface morphologies on both surfaces. Growth of TiO$_2$ on copper was observed with smaller growth rate than that on silicon but with similar surface morphology after bulk film formation, however, TiO$_2$ growth on copper surface
underwent nucleation with considerable delay before continuous film formation, which was not observed on silicon surface.
6. FUTURE WORK

During my PhD courses of research and study, different electrical characterization means such as CV/IV measurements have been utilized with helps from industry (DMC. J. Gordon). During those studies, it was found that there are pronounced hysteresis and frequency dispersions in some of the CV results, and those phenomena may be related to various reasons—trapped charges at interface; poor interface qualities between high-k films and silicon substrate or metal electrodes and high-k films; generated oxygen vacuums when doping with exotic materials, etc. In order to narrow down the pertinent parameters and understand how they are affecting the dielectric properties, controlled experiments must be designed. In future studies, emphasis on the electrical characterizations should be given.

Also, in my high-k research, it was found that by combining two different rare early materials it is possible to achieve high dielectric constants, but it also cause high leakage current densities in the composite metal oxide films—that is because crystalline phases will help to preserve a high “k” value while the leakage is more prone to drain along crystalline grains. So the question remains, how to achieve high dielectric constant while keep the leakage current density low? While, one the solution could be adding another amorphous barrier layer before growing the composite metal oxide; the barrier layer should be, first, also a high k material, second, amorphous in nature and could endure high temperature post deposition annealing, third, it should have good interface with silicon (should not react with silicon under deposition and annealing conditions); one the candidates meeting all above requirements is Al₂O₃. Upon optimization, it is
possible to design such a dielectric “super structure”, such as Hf\textsubscript{x}Ti\textsubscript{1-x}O\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3}/Si, which has very dielectric constant with suppressed leakage current densities.
CITED LITERATURE

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EDUCATION

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PUBLICATIONS

4. Q. Tao, G. Jursich and C. Takoudis, “Structural and Dielectric Characterizations of Atomic Layer Deposited HfO$_2$ and TiO$_2$ as Promising Gate Oxide”, Advanced Semiconductor Manufacturing Conference (ASMC) proceeding, Section 1, P 17-22 (2010)

TO BE SUBMITTED

1. Q. Tao, G. Jursich and C. Takoudis, “Investigation of Initial Growth of TiO$_2$ on Silicon and Copper Surfaces”
2. R. Xu, Q. Tao, Y. Yang and C. Takoudis, “Atomic Layer Deposition and Characterization of Erbium Oxide thin film On Si (100) Using (CpMe)$_3$Er Precursor and Ozone ”
3. Y. Yang, Q. Tao, C. Takoudis and G. Srinivasan, “Metaorganic Chemical Vapor Deposition of Multiferroic Composites-NiFe$_2$O$_4$ Thin Films on Piezoelectric Substrates ”

PRESENTATIONS

1. “Structural Characterizations of Atomic Layer Deposited HfO$_2$, TiO$_2$ and Hf$_x$Ti$_{1-x}$O$_2$ Using Tetrakis (diethylamino) precursors and H$_2$O”, American Institute of Chemical Engineers (AICHE) 2010 Annual Meeting, Salt Lake City, UT

3. “Structural and Dielectric Characterizations of Atomic Layer Deposited HfO$_2$ and TiO$_2$ as Promising Gate Oxide”, 21st Annual IEEE/SEMICON ASMC, San Francisco, CA, 2010

4. “Structural-Dielectric Property of Compositional Tuning of ALD Deposited YDH Oxide Films”, American Institute of Chemical Engineers (AICHE) 2009 Annual Meeting, Nashville, TN


**HONORS AND AWARDS**

1. 41st DAMOP Annual Meeting travel fellowship, Houston (2010)
2. GSC Travel Awards, University of Illinois at Chicago (2008, 2010)
4. University Merit Scholarship in Science & Engineering, Dalian University of Technology (2007)