UHF Radio Frequency Modules for Satellite-Ground Communication

BY

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Leonardo Maria Reyneri, Politecnico di Torino
To my family and all my loved ones

To redeem my dad Paolo and my brother Stefano who were less fortunate, but equally deserving

To thank those who supported me in school and life

To face the future with joy!
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<td>Abbreviation</td>
<td>Description</td>
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<td>---------------------------------------</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>AFC</td>
<td>Automatic Frequency Control</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>AraMiS</td>
<td>Modular architecture for Satellites</td>
</tr>
<tr>
<td>ASCII</td>
<td>American Standard Code for Information Interchange</td>
</tr>
<tr>
<td>ASK</td>
<td>Amplitude Shift Keying</td>
</tr>
<tr>
<td>AIS</td>
<td>Automatic Identification System</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistors</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary MOS</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial Off The Shelf</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
</tr>
<tr>
<td>CSMA</td>
<td>Carrier Sense Multiple Access</td>
</tr>
</tbody>
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<tr>
<th>Abbreviation</th>
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<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCE</td>
<td>Data Communication Equipment</td>
</tr>
<tr>
<td>DTE</td>
<td>Data Terminating Equipment</td>
</tr>
<tr>
<td>DSO</td>
<td>Digital Storage Oscilloscope</td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ESA</td>
<td>European Space Agency</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>FCS</td>
<td>Frame Check Sequence</td>
</tr>
<tr>
<td>FEC</td>
<td>Forward Error Correction</td>
</tr>
<tr>
<td>FOV</td>
<td>Field Of View</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency Shift Keying</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
</tbody>
</table>
| GENSO        | Global Educational Network for Satellite Opera-
<p>|              | tions                                          |
| GMSK         | Gaussian Minimum Shift Keying                   |</p>
<table>
<thead>
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<th>Abbreviation</th>
<th>Description</th>
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</thead>
<tbody>
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<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input/Output</td>
</tr>
<tr>
<td>HDLC</td>
<td>High Level Data Link Control</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>HBT</td>
<td>Hetero-junction Bipolar Transistor</td>
</tr>
<tr>
<td>HPBW</td>
<td>Half Power Beam-Width</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>ISI</td>
<td>Inter-Symbol Interference</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial, Scientific and Medical band</td>
</tr>
<tr>
<td>ITU-R</td>
<td>Radio-communication - International Telecommunication Unit</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>JPEG</td>
<td>Joint Photographic Experts Group</td>
</tr>
<tr>
<td>KISS</td>
<td>Keep It Simple, Stupid</td>
</tr>
<tr>
<td>LEO</td>
<td>Low Earth Orbiting</td>
</tr>
<tr>
<td>LFSR</td>
<td>Linear Feedback Shifted Register</td>
</tr>
<tr>
<td>LHCP</td>
<td>Left Hand Circular Polarization</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>MCU</td>
<td>Micro-Control Unit</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MIPS</td>
<td>Million Instructions Per Second</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>MSK</td>
<td>Minimum Shift Keying</td>
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<tr>
<td>NASA</td>
<td>National Aeronautics and Space Administration</td>
</tr>
<tr>
<td>NORAD</td>
<td>North American Aerospace Defense Command</td>
</tr>
<tr>
<td>NRZ</td>
<td>Non-Return to Zero</td>
</tr>
<tr>
<td>NRZI</td>
<td>Non-Return to Zero Inverse</td>
</tr>
<tr>
<td>OBC</td>
<td>On-Board Computer</td>
</tr>
<tr>
<td>OSI</td>
<td>Open Systems Interconnection</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAL</td>
<td>Phase Alternating Line</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PID</td>
<td>Protocol Identifier</td>
</tr>
<tr>
<td>PIFA</td>
<td>Planar Inverted F-Antenna</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
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<tr>
<td>--------------</td>
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<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>P-POD</td>
<td>Poly-PicoSatellite Orbital Deployer</td>
</tr>
<tr>
<td>PSK</td>
<td>Phase Shift Keying</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulator</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>QFN</td>
<td>Quad Flat No-leads package</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RAAN</td>
<td>Right Ascension of Ascending Node</td>
</tr>
<tr>
<td>RAID</td>
<td>Redundant Array of Independent Disks</td>
</tr>
<tr>
<td>RHCP</td>
<td>Right Hand Circular Polarization</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced Instruction Set Computer</td>
</tr>
<tr>
<td>RL</td>
<td>Return Loss</td>
</tr>
<tr>
<td>ROM</td>
<td>Read Only Memory</td>
</tr>
<tr>
<td>RSSI</td>
<td>Received Signal Strength Indication</td>
</tr>
<tr>
<td>RX</td>
<td>Receiver</td>
</tr>
<tr>
<td>SEE</td>
<td>Single Event Effects</td>
</tr>
<tr>
<td>SER</td>
<td>Symbol Error Rate</td>
</tr>
<tr>
<td>SEU</td>
<td>Single Event Upset</td>
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<thead>
<tr>
<th>Abbreviation</th>
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<tr>
<td>S/H</td>
<td>Sample and Hold</td>
</tr>
<tr>
<td>SHF</td>
<td>Super High Frequency</td>
</tr>
<tr>
<td>SIP</td>
<td>Single In-line Package</td>
</tr>
<tr>
<td>SMD</td>
<td>Surface-Mount Device</td>
</tr>
<tr>
<td>SME</td>
<td>Small Medium Enterprise</td>
</tr>
<tr>
<td>SMT</td>
<td>Surface-Mount Technology</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SOIC</td>
<td>Small Outline Integrated Circuit</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SPDT</td>
<td>Single Pole Double Throw</td>
</tr>
<tr>
<td>SRD</td>
<td>Short Range Device</td>
</tr>
<tr>
<td>SSID</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>THT</td>
<td>Through-Hole Technology</td>
</tr>
<tr>
<td>TID</td>
<td>Total Ionizing Dose</td>
</tr>
<tr>
<td>TL</td>
<td>Transmission Line</td>
</tr>
<tr>
<td>TNC</td>
<td>Terminal Node Controller</td>
</tr>
<tr>
<td>TX</td>
<td>Transmitter</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>--------------</td>
<td>--------------------------------------------</td>
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<tr>
<td>UHF</td>
<td>Ultra High Frequency</td>
</tr>
<tr>
<td>UML</td>
<td>Unified Modeling Language</td>
</tr>
<tr>
<td>USART</td>
<td>Universal Synchronous and Asynchronous Receiver/Transmitter</td>
</tr>
<tr>
<td>UTC</td>
<td>Coordinated Universal Time</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VEGA</td>
<td>Advanced Generation European Vehicle</td>
</tr>
<tr>
<td>VHF</td>
<td>Very High Frequency</td>
</tr>
<tr>
<td>VSWR</td>
<td>Voltage Standing Wave Ratio</td>
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This thesis is devoted to the development of a bidirectional telecommunication system for space applications. The module is going to be integrated in the AraMiS architecture, that is an innovative philosophy of small satellites based on tile-modularity and the use of low-cost commercial components.

The objective is to design the electronic board, the antenna apparatus and the control software to handle both the communication protocol and the housekeeping functions. According to the AraMiS specifications, the main constraints are collected in Table I.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Rate</th>
<th>$P_{TX \text{s}atellite}$</th>
<th>$P_{TX \text{ground}}$</th>
<th>Interface</th>
<th>On board supply</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>437 MHz</td>
<td>9.6 Kbps</td>
<td>33 dBm</td>
<td>47 dBm</td>
<td>SPI</td>
<td>[12 – 18] V, 15 W</td>
<td>165x165 mm$^2$</td>
</tr>
</tbody>
</table>

After an introduction referring to space-environment related issues and the state of the art in university satellites, the hardware design is carried out. Technical choices related to frequency selection, modulation and suitable equipment are taken and justified according to the power budget, project constraints and the availability of specific products on market. A set of devices is analyzed in terms of key-parameters in order to filter the most appropriate ones for each goal, then main block-schematics are provided. By means of specific CAD tools, both
schematics and PCB implementation are performed and depicted in the following chapters, then
the C++ control software is designed to drive the communication system, the processing unit
and all the housekeeping sensors. Since only COTS components are going to be used due to
the low-cost goal and those are neither space dedicated nor radiation robust, both protection
circuits and specific software routines must be implemented in order to keep electronic boards
in safe operating region. Such a precaution is fundamental to prevent the mission failure in
case of SEUs. After that, the propagation environment is studied and the most common UHF
radiating systems for satellite-ground communications are described. Finally, a suitable AraMiS
antenna and specific microwave circuits are designed to ensure both impedance matching and
high radiation efficiency in the band of interest.

In order to assure the system compatibility within the AraMiS framework and full technical
integration with the other subsystems, a UML description for the entire project documentation
is developed and steadily updated in the project library.
CHAPTER 1

INTRODUCTION

Space is a very challenging environment because of all the reasons which are going to be briefly described in the following sections. Especially regarding radiations, vibrations and partial vacuum related issues, specific countermeasures are used at both electronic and software design level. Those are going to be described in the chapters related to the components selection, the PCB implementation and the software architecture. Moreover, the state of the art in small satellites applications is also introduced. That makes the reader aware about the AraMiS background and provides information related to some academic prototypes already deployed. Since the thesis is devoted to the design of a telecommunication channel, specific technical reference coming from the state of the art ensures a safe starting point for the project.

1.1 Challenges of the space environment

1.1.1 Description

Satellites operate in conditions which are much different from terrestrial ones and the space environment is potentially hazardous to both humans and technical systems. As a matter of fact, it is populated by electrons and ionized atoms which are energy charged particles (cosmic rays or plasma) mainly emanated by the Sun through the solar wind or coming from the other stars. At high kinetic energies ($\sim$ MeV), these particles are sufficiently strong to ionize atoms
into the materials through which they propagate, while at lower energies ($\sim$ KeV) their effects range from charge accumulation on surfaces to the material degradation.

Earth’s surface is protected by the magnetosphere because it deflects most of the incoming charged particles through the action of the Lorentz force. The deflected charged particles form a plasma that is shaped in the form of a torus around the planet. This is known as Van Allen radiation belt and that is the reason why satellites must protect their sensitive components by means of adequate shielding, especially when they transit within that region for a long time. More precisely, the torus is split into two distinct belts which overall fill the space layers between 800 Km and 38000 Km above the Earth’s surface (energetic electrons form the outer belt, while a combination of protons and electrons form the inner one). Orbits positioned below the lower threshold (i.e. LEOs) ensure a high reduction in the probability of collisions between satellites and plasma stream[4].
Another element playing a key-role in the space environment is the presence of partial vacuum\cite{4}. Firstly, \textit{zero pressure} does not allow the use of components which include either pressurized gases or liquids (e.g. electrolytic capacitors, heat pumps) because they would produce explosions and evaporation. Secondly, the absence of any fluid filler leads to the impossibility of \textit{heat dissipation} by convection. As a consequence, inner electronic systems must be connected to the outer faces of the satellite by means of filling carbon-based materials in order to externally conduct thermal energy and dissipate it by \textit{irradiation}. Moreover, there is a huge \textit{thermal excursion} (even from 150 °C to −60 °C) between the faces which are illuminated by the sun and those in the shade. Regarding this, the smart way to cool all the faces exposed to the direct sunlight consists in generating electric power by means of photovoltaic panels.

In order to describe all the thermal contributions, the power balance of the satellite is now provided\cite{14}:
\[ \sum_i ((\alpha_i - \gamma_i) (F_S + F_T) S_i) - \sum_j (\alpha_j S_j) \sigma T^4 + P_{INT} + F_E \left( \alpha_{aff} S_{aff} + \alpha_{lat} \frac{S_{lat}}{2} \right) = mc \frac{dT}{dt} \]

where all the parameters are described in the following list.

- \(i\) is the index for all faces of the satellite which are directly illuminated by the Sun;
- \(j\) is the index for all faces of the satellite;
- \(F_S\) is the solar constant (1366 \(\text{W m}^{-2}\));
- \(F_T = F_s \alpha_T\) is the power density radiated by Earth as a consequence of the sunlight reflection;
- \(\alpha_T = 0.4\) is the mean terrestrial albedo;
- \(F_E = \sigma \alpha_T T^4 \left( \frac{R}{R+h} \right)^2\) is the power density radiated by Earth at a certain mean temperature;
- \(R\) is the Earth’s radius;
- \(h\) is the altitude of the orbit;
- \(S_{aff}\) is the area of the surface facing the Earth;
- \(S_{lat}\) is the area of the side surface (neither directly exposed to the sunlight, nor in the complete shade);
- \(\alpha\) is the absorbance of the material ([0,1]);
- \(\gamma\) is the efficiency associated to the photovoltaic panel ([0,1]);
• $\sigma$ is the Stefan-Boltzmann constant;

• $m$ is the mass of the satellite;

• $c$ is the specific heat capacity of the satellite;

• $P_{INT}$ is the thermal power produced by inner electric components;

• $S = S_{real} \sin(\theta)$ is the actual area which is exposed to the sunlight;

• $\theta$ is the sunlight incidence angle;

• $\frac{dT}{dt}$ is the infinitesimal temperature variation of the satellite.

Beyond thermal issues, space applications must also be safe from the oxidation phenomenon. It can heavily affect metal padstacks and connections due to the presence of monatomic oxygen orbiting at approximately $10 \text{ Km s}^{-1}$ in LEOs. As a matter of fact, even if satellites are surrounded by partial vacuum, just a small concentration of highly energetic oxygen is not negligible. In order to contrast such effect, gold metallizations should be adopted because they are stainless, but the overall cost of the system would increase too much. Since the target of the project is the development of a low-cost apparatus, it is preferable to prevent damages by means of external protections and subsystem redundancy.

Additionally, motion in space environment (e.g. orbit control) is totally assigned to expensive reaction engines. As a matter of fact, no supporting points are available, so there is no way to take advantage of friction force. Since propellant is limited, only few maneuvers can be performed and generally small satellites do not include a motion system. In contrast, reaction
wheels and magnetic actuators are often used for asset control which is not so expensive and can be adopted by all spacecrafts.

Finally, the strong acceleration of the launcher, the high temperature due to the friction with the atmosphere (up to 4000 °C) and vibrations during the launch (up to 60 g and up to 30 KHz for about 10’ when targeting 600 Km of altitude) put mechanical structures under dramatic stress at the very beginning of the space mission[14].

Figure 3 shows an example of a small orbital launch vehicle (4-stages and 30 m long system) developed by European Space Agency. The first stage is the one which provides the strongest acceleration since the weight to be moved is maximum: it is characterized by a thrust of 3040 KN and a burn time equal to 109.8 s[4].
1.1.2 Radiation effects

When incident radiations penetrate into a semiconductor solid material such as silicon, an electron-hole pair may be created if an electron in the valence band is excited into the conduction band. Electron-hole pairs generated in the gate oxide of MOS devices are separated by the electric field within the space charge region: electrons have high mobility, so they quickly drift away, while holes slowly drift in the opposite direction. Digital microcircuits are affected by such a phenomenon because trapped charges shift the MOS threshold voltage. Other influences may be the leakage current, time skew and logic-function failures. As time goes on, performance degrades because the total dose of radiation effects continuously increases and the system becomes slower and slower.

Uncontrolled charge generation can also lead to single-event effects which can be destructive (catastrophic device failure) or nondestructive (data and/or control losses).

Latch-up is the typical destructive case and it involves integrated circuits coming from CMOS fabrication processes. These chips inherently include parasitic BJTs formed by closely located structures that, under normal conditions, produce a n-channel and a p-channel transistors. A CMOS inverter can be used as an example and it is shown in Figure 4.

In the bulk cross-section it is possible to identify $R_S$, $R_W$ (both resistances are due to the intrinsic concentration associated to the inner layer) and the two parasitic bipolar transistors ($n$pn and $p$np)[14]. The equivalent circuit corresponds to a power electronic device called Silicon Controlled Rectifier (SCR) and can be reorganized as depicted in Figure 5.
Figure 4: CMOS inverter architecture with parasitics[14]

Figure 5: CMOS inverter equivalent circuit with parasitics (PSPICE)
The stable condition of the circuit implies the normal operating mode of the CMOS inverter and it holds when current does not flow through any of the two transistors. In contrast, whether a flux of electrons (generated as a consequence of radiation exposure) flows in one branch, a positive reaction arises and the circuit does not work properly anymore. As a matter of fact, if current $I_1$ flows, a voltage drop arises over $R_{HV}$, so that the base-emitter voltage related to the pnp transistor is no more negligible. Once it reaches $0.3 - 0.4$ V, such a transistor conducts, then there is a voltage drop across $R_S$ which leads the npn transistor in conduction mode too. Since $R_{HV}$ and $R_S$ are small resistances, the overall circuit basically acts as a short circuit between voltage supply and ground (the orange path in the schematic). That creates the destructive condition for the device due to Joule effect. The only available countermeasure is the adoption of an anti-latch-up circuit and that is basically a switch which detects the short-circuit condition and disconnects the voltage supply for a while[14].

On the other hand, the *up-set condition* is the typical nondestructive single-event effect. It consists in the change of logic state for a bistable element (typically a flip-flop) caused by the impact of either an energetic ion or proton.

As pointed out by Figure 6, the electric charges stored inside a node of a sequential system can vary due to an energetic-ion impact because it produces an ionization trace where charge accumulation arises (via drift/funneling and diffusion). That leads to the *bit-flipping phenomenon* and it implies corruption of the information previously stored. COTS components are not shielded against radiations, so the only countermeasure is to apply redundancy (different memory banks in different locations storing same data) and use protection codes to periodically
correct possible errors. The higher the circuit integration, the lower the amount of required charge to store a high logic level, the higher the probability to encounter errors.

1.2 State of the art in small satellites

1.2.1 CubeSat - U.S.A.

Avionics for satellites is a market which is continuously growing in these years thanks to both the availability of low cost launch-vectors and the efforts of industries and universities for developing their own satellites. In 1999, California Polytechnic State University and Stanford University created the CubeSat specifications and that helped the worldwide university communities in fostering space science and explorations[7]. The target was to build a really small satellite (10 cm-side cube) using low cost Commercial Off The Shelf components (COTS) that everybody could buy and assemble ad-hoc from a kit.
Nowadays, CubeSat standard is the state of the art in the field of low cost nano-satellites and its design philosophy currently allows universities to produce their own spacecrafts. The idea is to make students able to work on complex systems and become familiar with interdisciplinary problem-solving, as a result of deep cooperation among different engineering departments.

CubeSat specifications accomplish several high-level goals:

• Simplification of satellite infrastructure to produce a workable low cost spacecraft;

• Encapsulation of launcher-payload interface in order to take away the prohibitive amount of managerial work that would previously be required for matching the satellite with its launcher;

• Unification among payloads and launchers to enable quick exchanges of payloads and the use of launch opportunities on short notice.

The standard 10 cm-side basic CubeSat is often called "1U" meaning one unit. That conceptual definition is useful because CubeSats are scalable along one axis by 1U-block increments.
Since CubeSat faces are all 10x10 cm\(^2\) (regardless of the length, up to three units) they can all be launched and deployed using a common system called P-POD (Figure 8), still developed at California Polytechnic State University\(^[7]\). P-PODs are mounted to the launch vehicle and they carry CubeSats into orbit until the deployment command is received from the launcher.

Such a structure must avoid any possible collision among the small spacecrafts during the deployment procedure, so, once the aperture has been opened, a piston-spring pushes outside all CubeSats which are kept separated each other by means of additional intermediate springs.

Finally, it is possible to list the main requirements that CubeSat designers have to follow:

- Structure size must be coherent with the 1U basic block;
- Overall mass must be less than 1 Kg;
- The distance between the center of gravity and the geometric center cannot exceed 2 cm;
- External structure must be made of either Aluminum 7075 or Aluminum 6061-T6 in order to have the same P-POD thermal expansion;
• All edges of the mechanical structure must be rounded;

• Satellites must contain a general switch to activate all electronic systems during the deploying procedure, while it has to be turned off during launch;

• In order to avoid collisions with other satellites, antennas can be eventually extended out of the core structure only after few minutes from the deploying procedure;

• In order to avoid reciprocal interferences, ground-satellite transmissions can start only after few minutes from the deploying procedure;

• All the available power is supposed be provided by photovoltaic cells fixed on the outer faces;

• Propulsion systems are not allowed in order to avoid explosions during launch, so orbit control will not be possible.

1.2.2 **NCube - Norway**

NCube is a pico-satellite according to the CubeSat standard designed by four Norwegian universities in three years. Main mission purposes were[7]:

• Vessel traffic monitoring via satellite using the AIS system (which handles broadcast-signals transmitted by VHF transponders placed on the ships);

• Monitoring of reindeer herds (by equipping a few animals with transponders which allow to follow their movements);

• Testing of a new attitude control system based on active magnetic actuators (solenoids) and the passive gravitational gradient.
NCube is composed of three independent and fully testable subsystems which are the AIS units, the power management unit and the asset control unit.

In such a system, a key-role is played by a high-level ground station, placed at Svalbard islands by Norwegian Space Centre and consisting of 6 paraboloidal antennas. Those antennas can continuously keep in contact with the satellite, no matter of the occupied polar orbit (14 different orbits per day), so the data link is reliable.

A final remark regards the attitude control system because it consists of a standard magnetic actuation and a passive mechanical system. Firstly, current flowing through a solenoid generates a magnetic field which produces torque ($\tau$) as a result of interaction with the terrestrial magnetic field, according to the following law:

$$\tau \propto B_{Earth} \times B_{solenoid}$$
Beyond magnetic actuation (generally adopted for any small satellite), NCube makes also use of passive gravitational gradient.

This technique works on the gravity variation as a function of the position. If the axis of minimum inertia is oriented along the vertical direction (Nadir), the mechanical system is stable, so the asset control is determined. Otherwise, the satellite rotation takes place in order to reach the equilibrium point. As a matter of fact, satellites having elongated shape tend to orientate in such a way the radial axis coincides with the direction of protrusion.

### 1.2.3 AAU - Denmark

The AAU spacecraft is a pico-satellite developed at Aalborg University (AAU) according to the CubeSat standard[7]. Main targets were:
TABLE II: TELECOMMUNICATION FEATURES FOR NCUBE SATELLITE

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$P_{RX_{satellite}}$</th>
<th>Rate (GMSK)</th>
<th>Antenna</th>
<th>Protocol</th>
</tr>
</thead>
<tbody>
<tr>
<td>145 MHz</td>
<td>1 W</td>
<td>1.2/9.6 Kbps</td>
<td>Monopole</td>
<td>AX.25</td>
</tr>
<tr>
<td>162 MHz</td>
<td>1 W</td>
<td>1.2/9.6 Kbps</td>
<td>Monopole</td>
<td>AX.25</td>
</tr>
<tr>
<td>435 MHz</td>
<td>0.5 W</td>
<td>1.2/9.6 Kbps</td>
<td>Monopole</td>
<td>AX.25</td>
</tr>
<tr>
<td>2.2795 GHz</td>
<td>0.8 W</td>
<td>1.2/9.6 Kbps</td>
<td>Patch</td>
<td>AX.25</td>
</tr>
</tbody>
</table>

Figure 11: AAU satellite[7]

- to make engineering students closer to space applications;
- to acquire housekeeping-telemetry for evaluating system performance;
- to use a camera for scientific missions.

The satellite has been launched in June 2003 and a ground station having a paraboloidal antenna with 8 m-diameter was necessary to correctly implement the RF connection. The on-board antenna was a dipole and the data link connection was characterized by a bit-rate equal to 9.6 Kbps (GFSK modulated) at 437.475 MHz.
The result was not very successful because neither the complete telemetry has ever been received. The fault was likely due to a certain undetectable failure in the telecommunication system and to the wrong start-up power management. In the end, the functional requirements were not satisfied, but the experience pointed out some critical aspects that must be taken into account whenever a complex design is focused on an unreachable system. Firstly, test procedures in critical conditions are as important as the choice of the electronic components; secondly, unless a reliable radio link has been already established by the ground station (i.e. the full system control is ensured), it is better to associate only elementary functions to the satellite. The latter consideration is crucial to preserve the energy management and to avoid that the level of battery charge goes below the safety threshold for planning a recharge.

<table>
<thead>
<tr>
<th>TABLE III: TELECOMMUNICATION FEATURES FOR AAU SATELLITE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency</strong></td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>437.475 MHz</td>
</tr>
</tbody>
</table>
1.2.4 PicPoT - Italy

PicPoT project was born in 2004 at Polytechnic of Turin and its main goal was to develop an academic pico-satellite within the CubeSat framework. Unfortunately, it could not be tested because the launcher exploded during flight in July 2006. The set of specifications was:

- Cubic shape with 13 cm side;
- Mass equal to approximately 2.5 Kg;
- Power in TX-mode lower than 1.5 W;
- At least 90 days of life;
- LEO target;
- COTS electronic components;
- P-POD launcher compatible.

Initial mission requirements were to verify the reliability of COTS components in space applications, to take pictures of Earth from space, to exchange data with the ground station and to study the behaviour of GPS for LEO purposes.

The satellite incorporated two hot-redundant systems, each one with power management, latch-up controller, housekeeping, telemetry and telecommand facilities, one optical payload with three multispectral camera-systems (having JPEG compression and PAL encoding), together with a ground station placed on the roof of Polytechnic. The satellite was composed of 5 interacting processors, two independent half duplex RF links (one at 437 MHz with a dipole antenna and the other at 2.44 GHz with a PIFA), 5 solar panels which completely cover 4 outer
faces, 6 battery packs and was tested to be fully functional before launch. Moreover, a set of kill-switches was adopted to ensure the electric isolation of the satellite during the launch. That was in order not to waste energy or damage any component when the spacecraft was not yet deployed.

Redundancy was the key-idea in PicPoT project then, although the failure of a single component could happen, duplication of any subsystem allowed the satellite to still remain in working state. For instance, the telecommunication subsystem was based on two different physical channels (different frequency and antenna) and also the related processing units were differentiated: ProcA was based on Chipcon CC1010 transceiver and it handled a 9.6 Kbps data link with
output power equal to 35.7 dBm, while ProcB was based on MSP430 microcontroller and it handled a 10 Kbps data link with an output power of 30.8 dBm.

**TABLE IV: TELECOMMUNICATION FEATURES FOR PICPOT SATELLITE**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>( P_{TX_{\text{satellite}}} )</th>
<th>Rate (GMSK)</th>
<th>Antenna</th>
<th>Protocol</th>
</tr>
</thead>
<tbody>
<tr>
<td>437 MHz</td>
<td>1.2 W</td>
<td>9.6 Kbps</td>
<td>Helix</td>
<td>AX.25</td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>1.2 W</td>
<td>9.6 Kbps</td>
<td>Patch</td>
<td>AX.25</td>
</tr>
</tbody>
</table>
1.3 AraMiS

AraMiS (Italian acronym for “Modular Architecture for Satellites”) is a project (born at Polytechnic of Turin in 2007 and still going on) which goes beyond the CubeSat concept and aims to achieve a true modular architecture[2]. The general philosophy consists in developing reusable, modular, distributed and intercommunicating on-board units with COTS components. The system must be able to increase fault tolerance and allow a graceful performance degradation, while keeping the costs at acceptable levels. Moreover, the satellite can exhibit a versatile shape by means of as many basic modules as needed to perform the tasks of the mission. Since the same module design is used in several satellites, the AraMiS architecture achieves an effective cost sharing between different missions. As a matter of fact, the most effective way to reduce the cost of a nano or micro-satellite missions is to reduce as much as possible design and non-recurrent fabrication costs, which usually account for more than 90% of the overall budget. Design reuse is the rationale behind the AraMiS project and such principle requires to have a modular architecture focused on flexible and powerful module-tiles. Using the same structures more times obviously allows to share design, qualification and testing costs, then it can reduce the time-to-launch.

AraMiS includes a mechanical subsystem, a power management subsystem, a telecommunication subsystem, an on-board processing subsystem, the ground segment and the payload support. Most of the modular intelligent tiles have to be regularly placed on the outer surface of the satellite and have a double nature: both mechanical and functional. The inner part of the satellite is mostly left empty (except for the on-board processor and payload support tile), to
be filled by the user-defined payload, which is the only part to be designed and manufactured ad-hoc for each mission.

Figure 14 points out the presence of two outer tiles which are now briefly introduced.

- The power management tiles are mainly composed of a solar panel, a rechargeable battery to store energy, a battery charger, an active magnetic (solenoids) and/or inertial (reaction wheel) asset control and a microcontroller-based housekeeping module to keep track of voltages, currents and temperatures inside the tile;

- The telecommunication tiles are mostly composed of a microcontroller-based programmable transceiver, a 437 MHz or 2.44 GHz modem, a power amplifier for transmission, a low-noise amplifiers for reception and the antenna system. The user has not to take care of
any telecommunication detail, so all transmissions to/from the satellite must occur in a completely transparent manner;

The inner volume can be designed according to different typologies, but it is very useful to include the following tile.

• The On-board processor and payload support take care of all data handling for the user-defined payload. Such a tile has CPU power and memory, so that simple payloads may use it instead of having their own processor.

<table>
<thead>
<tr>
<th>TABLE V: ARAMIS TARGETING PERFORMANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
</tr>
<tr>
<td>---------------------------</td>
</tr>
<tr>
<td>Lifetime</td>
</tr>
<tr>
<td>Overall mass</td>
</tr>
<tr>
<td>TID</td>
</tr>
<tr>
<td>Orbit</td>
</tr>
<tr>
<td>Minimum size</td>
</tr>
<tr>
<td>Electronic components</td>
</tr>
<tr>
<td>Telecommunication channels</td>
</tr>
</tbody>
</table>

1.4 Global Educational Network for Satellite Operations (GENSO)

In the satellite-Earth communication field, GENSO is an ESA project approved in 2006 whose main goal is to realize a worldwide network of radio amateur and university ground stations to support the operations of university satellites. In order to achieve this goal, GENSO
has been designed as a distributed system connected via internet. The software applications
which facilitate the data sharing have been developed in Java by an international team of
students.

Mission controllers of university satellites can normally gather around 20 minutes of data
per day with their own university ground station. In contrast, GENSO will give them free access
to potentially hundreds of stations around the globe via internet and increase their data return
to many hours per day. It will also allow them to command their spacecraft from any side of
the world.

GENSO offers the capability to plan and schedule the use of ground station resources, to
predict the trajectories of spacecraft over the ground station and to automate tracking and
hardware control during a pass. The downlinked mission data is provided to the mission con-
trollers within a few minutes by the end of the pass, then real-time links for transmission of
telecommands and telemetry reception are also possible.

The AraMiS project has to comply with GENSO standard, so in the following paragraphs
the communication diagram is going to be described.

Whenever a Mission Control Client (MCC), such as the university that has built the space-
craft, needs to establish a connection with the satellite, it accesses through the internet link
to any of the Ground Station Server (GSS) located all over the world. This secure access is
controlled by the GENSO Authentication Server (AUS), which ensures at all times that the
entities participating in the network are allowed to do so. During a pass, any ground station
standing in the footprint receives data from the satellite and it is stored locally by the GSS.
Then the GSS notifies the AUS, which in turn notifies the MCC owning the satellite. Finally, the MCC can establish downlink/uplink sessions directly from the GSS. Since ground stations are physically placed all over the world, the satellite is automatically tracked and MCC can be connected with the spacecraft independently from its real position.

The datalink layer is based on the AX.25 amateur communication protocol (described later on), while the counterpart of the GSS inside the satellite is represented by the On Board Radio Frequency module (OBRF). In uplink operation, this module has to check for data correctness and both source/destination addresses, then it forwards the message to the On Board Computer (OBC). In downlink operation, OBC sends data to the OBRF and the latter subsystem builds the packet to be sent, then it transmits to ground.
CHAPTER 2

SYSTEM LEVEL DESIGN

After the previous introduction to the topic, the design procedure begins in this chapter. The first step consists in identifying the main electronic blocks which are going to constitute a suitable board for the UHF telecommunication subsystem. Each unit is initially considered as a black box, then all blocks are expanded in order to show details and relationships. Since no specific electronic device is introduced, but just functional features are considered, this chapter refers to the so called system design. Secondly, technical choices are taken regarding the frequency selection, the link budget and the modulation technique. As a matter of fact, those lead the reader to a complete system description because additional high level specifications integrate the initial AraMiS requirements.

2.1 Overall structure

The very top functional schematic associated to the telecommunication tile is shown in Figure 16.

The AraMiS core is connected to the telecommunication tile through a suitable interface which handles both data exchange and the power distribution. In principle, a single microcontroller unit should be shared by the two radio frequency channels (UHF and S-band) because, in the end, a single board will be used for both subsystems. Actually, since the thesis is only devoted to one communication channel, the S-band TX/RX unit will not be described in details.
Figure 16: Top-level block schematic

Figure 17: TX/RX-Unit block schematic
Figure 17 describes the UHF TX/RX unit, which is the telecommunication core. The transceiver has modulation/demodulation capability, it is fully managed by the microcontroller unit and it has two different paths for transmitting and receiving data streams. In the TX side, a power amplifier can be adopted to guarantee the desired output power, while in the RX side a low noise amplifier could be designed to increase the system sensitivity. Since only a single radiating element is planned for the application, the transceiver drives a radio frequency switch, which commutates between TX and RX mode in order to decouple the associated load impedances. As a remark, signals propagating from the transceiver to the antenna (and vice versa) are radio frequency ones, then connections must be designed as transmission lines to avoid reflections and mismatches.

Secondly, the microcontroller unit (Figure 18) basically contains an embedded programmable processor to manage the communication protocol, the housekeeping functionality (in terms of sensor-data recovery) and the interface with the AraMiS core. A JTAG connector must also be included in order to program and test the electronic board by means of a personal computer.
The switch unit is shown in Figure 19 and consists of three different kind of electrical switches. It contains a protection circuit to prevent latch-up damages, two main load switches to enable/disable either the entire board or just the power amplifier, then it includes a radio frequency switch for separating TX/RX data streams. The latter choice is due to the presence of a single shared antenna for both transmitting and receiving modes.

The AraMiS power distribution bus provides a variable voltage supply, while electronic devices generally need well defined and constant values. The power management unit (Figure 20) must then contain a switching converter for the higher current consumption devices (e.g.
power amplifier), while simpler linear regulators can be used to assure stable voltages for the low-consumption ICs (e.g. transceiver and microcontroller).

Finally, the housekeeping unit (Figure 21) is composed of a set of sensors which monitor currents, voltages and temperature. The related information are useful to check whether all the integrated circuits are correctly supplied and work in their safe operating regions. The temperature sensor is usually placed as close as possible to the most heat-sink device.

2.2 Frequency selection

The starting point in the physical implementation of a wireless channel is the frequency selection. Generally, a communication subsystem should work on two interchangeable frequency-separated channels for achieving fault tolerance. As a matter of fact, electromagnetic interference is frequency dependent, so providing two different paths for the same data stream (channel redundancy) ensures a more reliable communication.

In the AraMiS architecture, the first channel lays in the UHF band at 437 MHz, while the second one is in the S-band at 2.44 GHz. Such a frequency selection is basically due to
guarantee high spectral distance between the two homologue channels, so that they can be considered completely independent. Moreover, since the UHF channel belongs to the radio-amateur band (according to the *International Amateur Radio Union allocation*), data sharing among all radio-amateurs in the world is ensured and low-cost by definition. Similarly, the S-band channel benefits of the *Industrial, Scientific and Medical (ISM) radio bands* which are internationally unlicensed frequencies (2.4-2.5 GHz).

Consequently, the main advantage is that no additional money is required to use any of the two channels, but the drawback concerns the presence of noise coming from other electronic devices working in the same band, such as other radio-amateur transmissions and short-range wireless networks. A last remark about the ISM band refers to the output power: although the usual threshold is around 100 mW, much higher power levels (few watts) are tolerated inside the radio-amateur slot.

A further consideration regards the *Doppler effect* because it produces a relevant frequency shift in the band of interest ($\Delta f$). In fact, the working frequency increases when the satellite is approaching to the ground station, while it reduces in the other way round.

Figure 22 highlights the velocity component directed towards the receiver ($V_a = V \cos \alpha$) and such a vector is time varying since the satellite is supposed to travel on a circular orbit. At any time instant, the frequency variation is determined by the following equation[4]:

$$\Delta f = f_0 \frac{V_a}{c}$$

The worst case condition (i.e. $\Delta f$ is maximum) results when the spacecraft either rises or disappears on the horizon, since $V_a = V \cos \alpha \approx V \cos(0^\circ) = V = V_{a,max}$. 
TABLE VI: DOPPLER EFFECT OVER UHF AND S-BAND CHANNELS

<table>
<thead>
<tr>
<th>$f_0$</th>
<th>$\Delta f_{max}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>437 MHz</td>
<td>10.925 KHz</td>
</tr>
<tr>
<td>2.44 GHz</td>
<td>61 KHz</td>
</tr>
</tbody>
</table>

2.3 Link budget

Since the uplink power in transmission is defined as a project specification ($P_{TX_{ground}}$), it is possible to estimate the received power by means of the *noiseless Friis equation*. Such a step is mandatory to design a suitable receiver for the satellite application, because the received power must be greater than the sensitivity associated to the RX. A key-role is played by both TX/RX
antennas because their respective gains could heavily affect the final link budget. As a starting point, a dipole and a helix are respectively considered as transmitting and receiving antennas, while more specific radiating systems are going to be studied in the last sections of the thesis.

The linear formulation of the Friis equation is:

\[
P_{RX} = P_{TX} \cdot g_T(\theta, \phi) \cdot g_R(\theta, \phi) \cdot \chi(\theta, \phi) \cdot \alpha_{att} \cdot \alpha_{extra}
\]

where all the parameters are described in the following list.

- \(P_{RX}, P_{TX}\) are respectively the received and transmitted powers;
- \(g_T(\theta, \phi), g_R(\theta, \phi)\) are respectively the antenna gains as a function of the spherical angles (when expressed in dBi, the gain is compared to the isotropic radiator);
- \(\chi(\theta, \phi) = |\hat{p}_T(\theta, \phi) \cdot \hat{p}_R(\theta, \phi)|^2\) is the depolarization loss due to the polarization mismatch between the TX (\(\hat{p}_T\)) and RX (\(\hat{p}_R\)) antennas;
- \(\alpha_{att} = (4\pi R^2/\lambda^2)^{-2}\) is the free-space loss as a function of the wavelength (\(\lambda\)) and the distance between TX and RX (\(R\));
- \(\alpha_{extra}\) is the extra-attenuation loss and it keeps into account atmospheric absorption, fading, diffraction by obstacles and ground reflection.

A remarkable consideration is that Friis equation can be applied only in far field condition, that is TX and RX must be sufficiently far each other. Such a situation occurs when the following conditions are simultaneously met.
\[
\begin{align*}
R \gg \lambda & \quad \text{R is the TX-RX distance} \\
R \gg D & \quad \text{D is the maximum dimension of the antenna} \\
R > \frac{2D^2}{\lambda} & \quad \text{Fraunhofer criterion}
\end{align*}
\]

A rough analysis can be performed just by doing some assumptions:

- the refractive index is supposed to be constant and the entire system is surrounded by vacuum \((n = 1)\);
- the orbit is circular and the altitude is 600 Km (LEO);
- no external noise is introduced in the wireless communication;
- the antenna gains are supposed to be \(g_T(\theta, \phi) = 2\, dB\) (dipole, linear polarization) and \(g_R(\theta, \phi) = 15\, dB\) (helix, circular polarization);
- no extra-attenuation is taken into account;
- the Earth’s radius is constant and equal to \(t=6378\) Km;
- polarizations are constant (i.e. the ground station is supposed to be equipped by an automatic tracking system for keeping aligned the two antennas), but not fully matched (e.g. \(\chi = -3\) dB). A suitable pair of unit vectors representing such a scenario can be \(\hat{p}_T = \sqrt{\frac{2}{3}}(\hat{x} + \hat{y})\) and \(\hat{p}_R = \sqrt{\frac{2}{3}}(\hat{x} + j\hat{y})\).

The worst case condition arises when the satellite is in the position shown in Figure 23 (where \(p\) is the linear distance between the satellite and the ground station).
\[ p = \sqrt{(t + h)^2 - t^2} = \sqrt{2th + h^2} \approx 2831 \text{ Km} \]

Since the wireless link refers to a satellite communication, the far field condition is obviously met. As a matter of fact, \( h \) is the minimum distance between the satellite and the ground station and it is sufficiently large to avoid any near field analysis. Then it is possible to apply the Friis equation and compute the received power in worst case condition.

### 2.4 Data transmission issues

#### 2.4.1 Modulation techniques

Once the physical channel is defined in terms of frequency and link budget, the choice of a specific modulation becomes crucial. In fact, it defines how data is transmitted and a set of
### Quality parameters associated to the communication link

The main objectives when choosing a particular digital modulation are:

- high data rate;
- high spectral efficiency (minimum bandwidth occupancy);
- high power efficiency (minimum TX power);
- robustness against channel impairments (minimum bit error rate);
- low power/cost implementation.

Those are conflicting requirements, so the target is to identify the best tradeoff[4]. Firstly, the existing digital modulations can be classified in *linear* (information is associated to the signal amplitude/phase) and *nonlinear* (information is associated to the signal frequency).

Amplitude and phase modulations (*ASK, PSK, QAM*) are more susceptible to variations coming from fading and potential interference. Moreover, they both require the presence of linear amplifiers in order not to have distortion in the modulated signal. From the other point of view, a nonlinear modulation (*FSK*) has the advantage to allow the use of efficient nonlinear amplifiers and does not require coherent demodulation. As a matter of fact, amplitude nonlinearities do

---

**TABLE VII: LINK BUDGET**

\[ P_{TX} = 47 \text{ dBm (50 W)} \]

<table>
<thead>
<tr>
<th>LEO - altitude</th>
<th>( f ) [MHz]</th>
<th>( \lambda ) [cm]</th>
<th>( \alpha_{att} ) [dB]</th>
<th>( P_{RX} ) [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>600 Km</td>
<td>437</td>
<td>68.65</td>
<td>-154.3</td>
<td>-93.3</td>
</tr>
<tr>
<td>600 Km</td>
<td>2.44 GHz</td>
<td>12.5</td>
<td>-169.1</td>
<td>-108.1</td>
</tr>
</tbody>
</table>
not affect the user information and there is no need to synchronize the phase between TX and RX. The drawback is that frequency modulation generally leads to spectral broadening, then a lower spectral efficiency. Consequently, the latter technique is preferred to privilege robustness and power efficiency (typical benchmarks for satellite applications), while it is avoided when the main constraint is given by a narrow band channel.

Previous considerations lead to choose the FSK modulation as a compromise for the AraMiS framework. According to that technique, the modulated signal is going to have the following form[1]:

\[ s_i(t) = A \cos \left[ 2\pi f_c t + 2\pi \alpha_i \Delta f_c t + \phi_i \right], \quad 0 \leq t \leq T_s \]

where all the parameters are described in the following list.

- \( A \) is the constant envelope;
- \( T_s \) is the symbol duration;
- \( i \) is the index of the \( i \)-th message;
- \( f_c \) is the carrier frequency;
- \( 2\Delta f_c \) is the minimum frequency separation between two adjacent carriers within the modulation;
- \( \phi_i \) is the phase associated to the \( i \)-th carrier;
- \( \alpha_i = (2i - 1 - M) \), \( i = 1, 2, ..., M = 2^K \) is a coefficient;
- \( M \) is the number of available messages to be transmitted;
• $K = \log_2 M$ is the number of encoded bits into $s(t)$.

When the minimum frequency separation is $2\Delta f_c = \frac{0.5}{T_s}$, FSK is called MSK. That is the minimum possible frequency separation in FSK and therefore the modulation occupies the minimum bandwidth. Adopting MSK is a necessary condition to minimize the spectral inefficiency associated to the nonlinear modulation[1]. Furthermore, pulse shaping can give a great contribution to the good use of the frequency spectrum and the Gaussian shape is the most diffused one with the FSK technique (e.g. GSM standard for digital cellular system). The Gaussian shape is defined as:

$$g(t) = \frac{\sqrt{\pi}}{\alpha} e^{-\left(\frac{\pi t}{\alpha}\right)^2} \leftrightarrow G(f) = e^{-(\alpha f)^2}$$

The larger $\alpha$, the better the spectral properties, but the higher the ISI.

2.4.2 constellation and Bit Error Rate

After the modulation technique is determined, the constellation size must be chosen. For linear modulations, it must be considered that the larger the constellation, the higher the data rate for a given bandwidth, the lower the robustness. In FSK there is a significant difference regarding the constellation size because, as far as it increases, for any given bit-rate the required bandwidth becomes larger. As a matter of fact, the Shannon bandwidth is defined as follows.

$$W_{Sh} = \frac{N_d}{2T_s} = \frac{M}{2T_s} = \frac{R_b M}{2\log_2 M}$$
where \( N_d \) is the number of dimensions related to the constellation, \( M \) is the number of available symbols, \( T_s \) is the symbol duration and \( R_b \) is the bit-rate. The goal is to minimize \( M \) in order to achieve the simplest modulator/demodulator scheme and the highest possible spectral efficiency. However, \( M \) must also ensure a reliable data link with a sufficiently high level of robustness (low BER).

The symbol error rate is computed as [1]:

\[
SER = P_s = 1 - \sum_{k=0}^{M-1} (-1)^k \binom{M - 1}{k} \frac{1}{k + 1} e^{-\frac{k}{k + 1} \gamma_s}
\]

In case of Gray encoding, the bit error rate is:

\[
BER \approx \frac{P_s}{\log_2 M}
\]

where all the parameters are described in the following list.

- \( M \) is the number of available symbols;
- \( \gamma_s = \frac{E_s}{N_0} \), where \( E_s \) is the per symbol energy and \( N_0 \) is the noise power spectral density;
- \( E_s = E_b \log_2 M \) and \( N_0 = K_b T \), where \( E_b \) is the per bit energy, \( K_b \) represents the Boltzmann constant and \( T \) is the equivalent temperature;
- \( T = T_A + T_{eqRX} = T_A + T_{REF} (F - 1) \), where \( T_A \) is the temperature of the antenna (a worst case estimation can be 450 K), \( T_{eqRX} \) is the equivalent temperature at the receiver, \( F \) is the noise figure associated to the receiver and \( T_{REF} \) is the reference temperature at which \( F \) has been estimated by the manufacturer;
• $SNR = \frac{P_{RX}}{N_0B_i}$ is the signal to noise ratio at the receiver considering the worst case noise power density and the bandwidth of the filter at the receiver ($B_i$).

A MATLAB script has been implemented to show the quality parameters associated to the FSK modulation in the UHF band. Results are collected in Table VIII.

```matlab
% % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % %
% Communication parameters for FSK modulation in the UHF band %
% % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % %

clear all

M=8; %Maximum number of symbols to be analyzed

FdB=10; %Noise figure of the receiver (dB)

Ta=450; %Maximum temperature of the antenna (K)

Tref=290; %Reference temperature associated to F (K)

KB=1.3806503e-23; %Boltzmann constant

PdB=-93.3; %Received power (dBm)

Ppenalty=15; %Additional losses due to interference (dB)

Bi=12500; %Bandwidth of the filter at the receiver (Hz)
```
Prx = 10^((PdB−Ppenalty)/10)/1000;

F = 10^((FdB/10));

T = Ta + Tref*(F−1);

No = Kb*T;

for a=2:M
    mat(a−1,1)=a; \text{\%Number of symbols}
    mat(a−1,2)=Rb*a/(2*log2(a)); \text{\%Shannon bandwidth}
    mat(a−1,3)=log2(a); \text{\%Number of bits}
    SNRsh=Prx/(No*mat(a−1,2)); \text{\%SNR matched on the Shannon bandwidth}
    SNR=Prx/(No*Bi); \text{\%SNR matched on the actual RX bandwidth}
    mat(a−1,4)=10*log10(SNRsh); \text{\%SNRsh (dB)}
    mat(a−1,5)=10*log10(SNR); \text{\%SNR (dB)}
    gamma=Prx*log2(a)/Rb/No;
    tmp=0;
    for (k=0:a−1)
        tmp=tmp+(-1)^(k)*choosek(a−1,k)/(k+1)*exp(-k*gamma/(k+1));
    end
    mat(a−1,6)=1−tmp; \text{\%Symbol error rate (SER)}
    mat(a−1,7)=mat(a−1,6)/mat(a−1,3); \text{\%Bit error rate (BER)}
In order to have worst case estimations, an additional loss equal to 15 dB is considered to take into account interference, extra-attenuation and non-idealities. Moreover, the noise figure associated to the receiver is assumed to be 10 dB (measured at a reference temperature of 290 K). In Table VIII, $SNR_{W_{Sh}}$ is the signal-to-noise ratio computed over the Shannon bandwidth, while $SNR_{B_i}$ is the ratio computed over the actual bandwidth associated to a real receiver (TI-CC1020).

<table>
<thead>
<tr>
<th>$M$</th>
<th>$W_{Sh}$ [KHz]</th>
<th>bits/symbol</th>
<th>$SNR_{W_{Sh}}$ [dB]</th>
<th>$SNR_{B_i}$ [dB]</th>
<th>SER</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>9.6</td>
<td>1</td>
<td>15.62</td>
<td>14.47</td>
<td>6.02 · 10^{-9}</td>
<td>6.02 · 10^{-9}</td>
</tr>
<tr>
<td>4</td>
<td>9.6</td>
<td>2</td>
<td>15.62</td>
<td>14.47</td>
<td>2.22 · 10^{-16}</td>
<td>1.11 · 10^{-16}</td>
</tr>
<tr>
<td>8</td>
<td>12.8</td>
<td>3</td>
<td>14.37</td>
<td>14.47</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Previous data point out that the higher $M$, the higher the performance in terms of $SNR$ and $BER$. In contrast, the Shannon bandwidth proportionally increases with the number of symbols. Then, since $R_b$ is constant, the higher $M$, the worse the spectral efficiency. However,
BER is sufficiently small in any situation ($< 10^8$), so the best compromise in the UHF band can be given by the simplest constellation ($M = 2$).

As a result, the final choice is going to be the 2-FSK/GFSK modulation.
CHAPTER 3

PARTS SELECTION

According to the results coming from the system level design and the AraMiS requirements, a set of suitable electronic devices can be detected (i.e. main ICs and the associated passive networks). The selection is performed within the products which are available on the market, then the related operation principles are described. In this context, some precautions regarding the components selection are taken according to the space related issues.

3.1 Transceivers

3.1.1 UHF channel device selection and description

Table IX points out the main requirements for the transceiver unit. They have been previously identified, so now they are just collected for convenience.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Rate</th>
<th>$P_{TX_{satellite}}$</th>
<th>On board supply</th>
<th>$P_{RX_{satellite}}$</th>
<th>Modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>437 MHz</td>
<td>9.6 Kbps</td>
<td>33 dBm</td>
<td>[12 – 18] V, 15 W</td>
<td>-93.3 dBm</td>
<td>FSK/GFSK</td>
</tr>
</tbody>
</table>

Then, a set of commercial transceivers is analyzed in terms of frequency band ($B$), sensitivity ($S$), current consumption in receiving mode ($I_{RX}$), supply voltage ($V_s$), maximum TX power
(\(P_{TX}\)), maximum data-rate \(R_b\), kinds of supported modulations, working temperature range \(T\), microcontroller \(\mu C\) and price. The goal is to identify which one can be used for the AraMiS application and any incompatibility is marked (Table X).

| TABLE X: COLLECTION OF PARAMETERS ASSOCIATED TO DIFFERENT COMMERCIAL IC TRANSCEIVERS |
|---------------------------------|-----|-----|-----|-----|-----|
|                                | CC1020 | MC12311 | CC1000 | SX1211 | CC1101 |
| \(B\) [MHz]                   | 402 to 470 | 315 to 960 | 300 to 1000 | 863 to 870 | 387 to 464 |
| \(S\) [dBm]                   | -118 | -120 | -110 | -107 | -112 |
| \(I_{RX}\) [mA]               | 19.9 | 16 | 7.4 | 3 | 14 |
| \(V_s\) [V]                   | 2.3 - 3.6 | 1.8 - 3.6 | 2.1 - 3.6 | 5.0 | 1.8 - 3.6 |
| \(P_{TX}\) [dBm]              | 10 | 17 | 10 | 12.5 | 12 |
| \(R_b\) [Kbps]                | 153.6 | 1.2 | 76.8 | 25 | 500 |
| FSK                            | yes | yes | yes | yes | yes |
| GFSK                           | yes | yes | no | no | yes |
| \(T\) [°C]                    | -40 to 85 | -40 to 85 | -40 to 85 | -40 to 85 | -40 to 85 |
| \(\mu C\)                     | no | included | no | no | no |
| Price [$]                      | 1.56 | 2.80 | 1.80 | 1.90 | 2.00 |

The final choice for the UHF radio link is the transceiver *Texas Instruments/Chipcon CC1020*. This is a single-chip unit and implements a complete digital radio with one output and one input channel\[15\]. Moreover, such a transceiver shows good sensitivity and a programmable TX power level. Although that is the most suitable IC, it has a limited output power and does not include any processing unit, so it is necessary to add two subsystems in the communication chain. Firstly, a *microcontroller* must be connected for providing both interface capability and
packets management, then a *power amplifier* (PA) must be included at TX side to ensure the expected output power. Since sensitivity is sufficiently high when compared to the received power, there is no need of a *low noise preamplifier* (LNA) at the RX side. However, a suitable LNA is going to be defined in order to provide a suitable reference for possible future extensions.

Additionally, a *SPDT switch* is used to interface the antenna with either the PA-output or the LNA-input in order to decouple the TX/RX networks (Figure 24). The SKY13290-313LF unit is a suitable RF switch because it is based on the pHEMT technology and shows lots of advantages. As a matter of fact, it requires low control voltages and provides high isolation, low insertion loss and ultra-miniature package size.

According to the top-down approach, once the transceiver has been selected a deeper analysis can be carried out to study how it works. The CC1020 functional diagram is shown in Figure 25[15].

![Figure 24: UHF communication chain](image)
The received radio signal is amplified by means of two LNAs. The first one has a fixed gain, while the second LNA is a variable gain amplifier. The latter allows to keep constant the output power level according to the amplitude of the input signal. After that, the analog signal is down converted in phase/quadrature (I and Q) at the intermediate frequency (IF), then it reaches the ADC. In this chain, the automatic gain control, the fine channel filtering, the digital demodulation and the bit synchronization are performed digitally. Moreover, in order to match the input signal range to the whole dynamic of the ADCs, a variable gain amplifier is placed just before each converter. Such a precaution is necessary to minimize the quantization noise. In the end, the digital output is available at DIO pin, while the corresponding synchronous clock signal is returned on DCLK.
In TX mode, the RF output is frequency shift keyed by the digital bit-stream coming from the DIO pin. The integrated circuit contains a single frequency synthesizer which is shared by the RX/TX chains, so it generates both the signals for down-converting the input analog stream and the final RF output signals. The expected frequencies are digitally programmed and they are achieved by means two dividers. Optionally, a Gaussian filter can be used to obtain the Gaussian FSK modulation (GFSK).

The frequency synthesizer includes a complete on-chip VCO operating in the range between 1.608 GHz and 1.880 GHz. Then, a 90° phase splitter allows to generate the LO_I and LO_Q signals for the two down-conversion mixers (RX mode). The CHP_OUT pin is the charge pump output and VC is the voltage control node associated to the VCO. The external loop filter of the PLL chain is placed between these pins and a crystal must be connected between XOSC_Q1 and XOSC_Q2 to provide a reference clock signal.

PA_EN and LNA_EN are output pins which can be optionally used to enable/disable external PA/LNA stages. PDO, PDI, PCLK and PSEL are the module digital interface and they are going to be described later on.

Additional features on the specific transceiver are shown in Table XI and Table XII.

The CC1020 integrated circuit intrinsically needs external passive components in order to set up the PLL in the band of interest. Moreover, specific matching/filtering networks are required to ensure noise rejection and avoid power waves reflection. The corresponding parts selection is figured out by means of the Chipcon SmartRF Studio tool.
Figure 26: Screen shot of SmartRF Studio
TABLE XI: ADDITIONAL DETAILS FOR CC1020

<table>
<thead>
<tr>
<th>TX</th>
<th>Encoding (max data rate)</th>
<th>NRZ (153.6 Kbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FSK Binary frequency separation</td>
<td>108 KHz</td>
</tr>
<tr>
<td></td>
<td>Programmable output power</td>
<td>−20 dBm to 10 dBm</td>
</tr>
<tr>
<td></td>
<td>Optimum load impedance at TX pin</td>
<td>(54 + j44) Ω</td>
</tr>
<tr>
<td></td>
<td>Load impedance with matching network</td>
<td>50 Ω</td>
</tr>
<tr>
<td></td>
<td>2nd and 3rd harmonics</td>
<td>−50 dBc</td>
</tr>
<tr>
<td></td>
<td>$I_{TX}$ at maximum output power</td>
<td>27.1 mA</td>
</tr>
<tr>
<td>RX</td>
<td>Channel spacing</td>
<td>12.2 KHz</td>
</tr>
<tr>
<td></td>
<td>Intermodulation rejection</td>
<td>30 dB</td>
</tr>
<tr>
<td></td>
<td>Load impedance with matching network</td>
<td>50 Ω</td>
</tr>
<tr>
<td></td>
<td>Intermediate frequency</td>
<td>307.2 KHz</td>
</tr>
<tr>
<td></td>
<td>Digital filter bandwidth</td>
<td>9.6 KHz to 307.2 KHz</td>
</tr>
</tbody>
</table>

TABLE XII: PLL AND CLOCK SPECIFICATIONS FOR CC1020

<table>
<thead>
<tr>
<th></th>
<th>Phase Noise</th>
<th>−90 dBc/Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bandwidth</td>
<td>2.7 KHz</td>
</tr>
<tr>
<td></td>
<td>Lock Time</td>
<td>900 μs</td>
</tr>
<tr>
<td></td>
<td>Turn ON time</td>
<td>3.2 ms</td>
</tr>
<tr>
<td></td>
<td>Crystal Oscillator Frequency</td>
<td>14.7456 MHz</td>
</tr>
</tbody>
</table>

At 437 MHz, the T-type topology is used for impedance matching and filtering purposes in the TX branch. The corresponding set of components is described in Figure 27 and Table XIV. Furthermore, DC bias is provided to the RF_OUTPUT pin through L2, while C3 and C60 act as clamping components for DC and RF signals respectively. Similarly, L1 and C1 work as main filter network for the RX branch [15].
TABLE XIII: PASSIVE COMPONENTS SELECTION FOR CC1020

<table>
<thead>
<tr>
<th>Branch</th>
<th>ID</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX</td>
<td>$L_1$</td>
<td>33 nH</td>
</tr>
<tr>
<td></td>
<td>$C_1$</td>
<td>10 pF</td>
</tr>
<tr>
<td></td>
<td>$C_3$</td>
<td>5.6 pF</td>
</tr>
<tr>
<td></td>
<td>$L_2$</td>
<td>22 nH</td>
</tr>
<tr>
<td></td>
<td>$R_{10}$</td>
<td>82 Ω</td>
</tr>
<tr>
<td></td>
<td>$C_{60}$</td>
<td>220 pF</td>
</tr>
<tr>
<td>TX</td>
<td>$C_3$</td>
<td>5.6 pF</td>
</tr>
<tr>
<td></td>
<td>$R_{10}$</td>
<td>82 Ω</td>
</tr>
<tr>
<td></td>
<td>$C_6$</td>
<td>56 nF</td>
</tr>
<tr>
<td></td>
<td>$C_7$</td>
<td>2.2 nF</td>
</tr>
<tr>
<td></td>
<td>$C_8$</td>
<td>560 pF</td>
</tr>
</tbody>
</table>

Figure 27: CC1020 Input/Output matching network[15]

As shown in the screen shot (Figure 26), CC1020 is optimized to work with a 14.7456 MHz crystal having accuracy equal to ±5 ppm. Since there are no commercial crystals able to provide a so accurate frequency, in order to meet those specifications a digital external oscillator is going to be adopted. The FOX924B oscillator produced by FOX ELECTRONICS is the final choice because it shows wide temperature range ([-40, 85] °C) and high frequency stability (±5 ppm). The latter is crucial to ensure a consistent design because the frequency accuracy must not
TABLE XIV: PASSIVE COMPONENTS COMPONENTS SELECTION FOR THE CC1020 T-TYPE FILTER

<table>
<thead>
<tr>
<th>ID</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C72</td>
<td>4.7 pF</td>
</tr>
<tr>
<td>L70</td>
<td>47 nH</td>
</tr>
<tr>
<td>L71</td>
<td>39 nH</td>
</tr>
</tbody>
</table>

exceed the frequency shift due to the Doppler effect. The following computation proves that such a condition is fully verified.

$$\Delta f_{osillator} = \frac{5}{10^6} 14.7456 \text{ MHz} = 73.728 \text{ Hz} \ll \Delta f_{Doppler} = 10.925 \text{ KHz}$$

Finally, the manufacturer provides a reference design for decoupling capacitors and power supply filtering (Figure 28 and Table XV). At this regard, decoupling capacitors supply current peaks when CMOS digital circuits change their logic state, so they must be located as close as possible to the corresponding pin in order to limit parasitics.

Electromagnetic interference (i.e. AC components) over the supply network is tackled by using a ferrite bead (L21), that shows a frequency dependent impedance. Resistance is associated to the physical dimensions of the metal, while reactance is due to its inductive behaviour. At low frequency, the inductive impedance is low, while as frequency increases the overall impedance goes up. As a result, the component acts as an open circuit for radio frequency signals allowing DC current flow and blocking RF. Additionally, AC signals are attenuated because they induce eddy currents inside the bead and the corresponding power is dissipated due to the Joule effect.
Figure 28: Power supply filtering and decoupling network for CC1020[15]

Figure 29: Example of behaviour for a bead component
Regarding the passive components selection, a last remark concerns the ceramic capacitors listed in Table XV. The main difference among their dielectrics is the temperature coefficient. NP0 stands for “negative-positive-zero” (i.e. ±0) and capacitors labeled with such a tag are made of dielectrics which show the lowest change in the temperature coefficient (typical values range from 1 pF to 100 nF with 5% tolerance). This parameter gives information about how much the capacitance changes as a function of temperature, so that it is related to the component stability. The X7R tag is associated to less stable capacitors, but still good for non-critical coupling branches (typical values range from 100 pF to 22 µF with 10% tolerance).

All details related to the CC1020 package and the complete pins description are collected in Appendix A[15]. Furthermore, for the application circuit and the external components description, see Appendix B.

<table>
<thead>
<tr>
<th>ID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C46, C36</td>
<td>68 pF, 0402, NP0</td>
</tr>
<tr>
<td>C10</td>
<td>10 µF, 1206, X7R</td>
</tr>
<tr>
<td>C47</td>
<td>33 pF, 0402, NP0</td>
</tr>
<tr>
<td>C41</td>
<td>10 nF, 0402, X7R</td>
</tr>
<tr>
<td>C40</td>
<td>12 pF, 0402, NP0</td>
</tr>
<tr>
<td>C52</td>
<td>150 pF, 0402, NP0</td>
</tr>
<tr>
<td>C39</td>
<td>220 pF, 0402, NP0</td>
</tr>
<tr>
<td>C38, C90, C94</td>
<td>1 nF, 0402, X7R</td>
</tr>
<tr>
<td>R8</td>
<td>33 Ω, 0402</td>
</tr>
<tr>
<td>L21</td>
<td>1 KΩ, EMI filter ferrite bead</td>
</tr>
<tr>
<td>L22</td>
<td>1.2 nH, 0402</td>
</tr>
</tbody>
</table>
3.1.2 S-band channel device selection and description

Similarly to the UHF channel, a parallel research for suitable commercial transceivers is performed for the S-band branch. As previously mentioned, the thesis is only focused on the 437 MHz frequency, but this analysis is carried out for possible future expansions.

<table>
<thead>
<tr>
<th>TABLE XVI: TX/RX SPECIFICATIONS IN THE S-BAND CHANNEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
</tr>
<tr>
<td>2440 MHz</td>
</tr>
</tbody>
</table>

Table XVI highlights the technical specifications to be met, while Table XVII collects the TX/RX units which have been identified (any incompatibility with the AraMiS requirements is marked).

The best compromise for the S-band radio link is the transceiver Texas Instruments/Chipcon CC2510F32[16]. In fact, all the devices which have been analyzed require an external LNA because their sensitivity is too low, but LMX3162 is just a receiver, while CC2500 does not include the microcontroller. In contrast, CC2510F32 incorporates both a complete radio modem and a processing unit (including 32 KB of programmable flash memory and 4 KB of RAM).

The drawback associated to such a chip is that the RF input and the RF output pins are not separated. As a consequence, in order to decouple the TX/RX paths and reduce parasitic
TABLE XVI: COLLECTION OF PARAMETERS ASSOCIATED TO DIFFERENT COMMERCIAL S-BAND IC TRANSCEIVERS

<table>
<thead>
<tr>
<th></th>
<th>CC2500</th>
<th>CC2510F32</th>
<th>LMX3162</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B$ [GHz]</td>
<td>2.4 to 2.4835</td>
<td>2.4 to 2.4835</td>
<td>2.4 to 2.4835</td>
</tr>
<tr>
<td>$S$ [dBm]</td>
<td>-104</td>
<td>-103</td>
<td>-93</td>
</tr>
<tr>
<td>$I_{RX}$ [mA]</td>
<td>13.3</td>
<td>14.7</td>
<td>50</td>
</tr>
<tr>
<td>$V_s$ [V]</td>
<td>1.8 - 3.6</td>
<td>2 - 3.6</td>
<td>3 - 5.5</td>
</tr>
<tr>
<td>$P_{TX}$ [dBm]</td>
<td>1</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>$R_b$ [Kbps]</td>
<td>500</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td>FSK</td>
<td>yes</td>
<td>yes</td>
<td>-</td>
</tr>
<tr>
<td>GFSK</td>
<td>yes</td>
<td>yes</td>
<td>-</td>
</tr>
<tr>
<td>$T$ [$^\circ$C]</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
<td>-10 to 70</td>
</tr>
<tr>
<td>$\mu C$</td>
<td>no</td>
<td>included</td>
<td>no</td>
</tr>
<tr>
<td>Price [$$]</td>
<td>1.40</td>
<td>2.45</td>
<td>0.48</td>
</tr>
</tbody>
</table>

impedances, the most convenient solution consists in using two identical devices, one as a receiver and the other as a transmitter.

Since the maximum output power is not sufficient, an external power amplifier must be added on the TX branch and a suitable device can be the RFMD RF5152 (gain of 34 dB in the band of interest). Similarly to the UHF channel, the power amplifier would not work in its linear region, but this is not a problem because both FSK and GFSK modulations are independent from the signal amplitude. Finally, at the RX side a low noise amplifier is required to increase the sensitivity and a possible device which matches the requirements is the Kuhne 2227A. As a matter of fact, it would improve the system sensitivity to $-129$ dBm (gain of 25 dB and a low noise figure equal to 1.2 dB).
Once the transceiver has been selected, a deeper description of the integrated circuit can be performed. The functional diagram associated to the CC2510F32 is shown in Figure 31.

Firstly, the transceiver is naturally designed to work with differential wired transmissions because its interface includes both the positive and the negative RF signals (RF\_P and RF\_N). However, for a wireless radio link it is possible to use just a single pin.

At the RX side, RF signals are amplified by a low noise variable-gain amplifier, then they are down-converted in phase/quadrature (I and Q) at the intermediate frequency. After that, the I/Q signals are converted by the ADCs and they are digitally demodulated. Similarly to the CC1020, the automatic gain control, the fine channel filtering and the bit/packet synchronization are digitally performed.

From the other point of view, the TX branch is based on the direct synthesis of RF signals. The synthesizer includes a complete on-chip VCO and a 90° phase shifter for generating both
the LO_I and LO_Q signals to the down-conversion mixers (RX mode). A high speed crystal oscillator generates the reference frequency for the synthesizer, as well as the clock signals for the ADCs and the digital units.

Graphical details related to write/read operations and the corresponding timing description are available in Appendix C.

3.2 Microcontroller in the UHF channel

3.2.1 Interface

As previously mentioned, the CC1020 transceiver must be interfaced to an external processing unit. A suitable microcontroller should be able to:
• program the CC1020 into different configuration modes via the 4-wires serial interface (PDI, PDO, PCLK and PSEL);

• communicate through the bidirectional synchronous data interface (DIO for data exchange and DCLK for synchronization);

• perform packet assembly/disassembly;

• check for addresses and CRC;

• monitor the LOCK pin associated to the PLL frequency lock status;

• read back the RSSI value and other status information via the 4-wire serial interface.

CC1020 is configured through a 4-wires SPI-compatible interface where the transceiver is set as a slave device. It contains 8-bit configuration registers and they are addressed by 7-bit strings. A full CC1020 configuration requires 33 data frames where each frame is 16 bits long.
(7 address bits, R/W bit and 8 data bits) and the time needed for the complete configuration depends on the PCLK frequency.

During each writing cycle, 16 bits are sent on the PDI-line. The seven most significant bits of each data frame (A6:0) are the addressing bits and the MSB is sent as the first one. The next bit is the R/W bit (1-logic for writing, 0-logic for reading), then 8 data bits are transferred (D7:0). During address and data transferring, the PSEL signal (Program SE lect) must be 0-logic. Registers can be programmed in any order and the configuration data will be retained during a programmed power down mode, but not when the power supply is turned off.

The configuration registers can also be read by the microcontroller via the same configuration interface. In this case, the seven addressing bits are firstly sent, then the R/W bit must be set to 0-logic in order to initiate the data read-back. At this point, CC1020 returns data from the addressed register and PDO is used as a data output pin, so it must be configured as an input for the microcontroller. The PDO signal is set at the negative edge of PCLK and should be sampled at the positive edge, while PSEL must be set high between each read/write operation.

3.2.2 TI-MSP430 family and the old MSP430F1121A

The Texas Instruments MSP430 family of ultra low-power microcontrollers has been selected as a reference type of processing units for the AraMiS framework. That is because MSP430 combines low-power consumption with sufficiently high performance in terms of peripherals, MIPS and GPIO pins. The architecture is built around a 16-bit RISC CPU and supports five low power modes which allow to extended the battery life (the current consumption in the idle mode can be even less than 1 µA). Generally, all the MSP430 series processors are intended
for low cost and low power consumption embedded applications, so they are suitable for the AraMiS telecommunication subsystem.

In this specific context, the microcontroller has to:

- exchange commands, telemetry and packets with the OBC;
- assembly/disassembly packets by performing scrambling/descrambling, bit-stuffing and insertion of header information;
- check for addresses and CRC correctness;
- control and program the transceiver;
- manage the housekeeping sensors;
- control the power management.

The \textit{MSP430F1121A} is a MSP430 series processor which was selected for the implementation of other AraMiS subsystems. Its main features are collected in Table XVIII and they directly point out the main advantages of using the MSP430 family\cite{17}.

As shown in Figure 33, the CPU is integrated with 16 registers, 16-bit core buses and 14 I/O ports with interrupt capability. The architecture provides reduced instruction execution time and the register-to-register operations are all one clock-cycle long for an easy pipeline scheduling. As shown in Figure 34, there are seven addressing modes for source operands and four addressing modes for destination ones. Moreover, just four registers (R0 to R3) are dedicated (program counter, stack pointer, status register, and constant generator), while all the remaining ones are general-purpose.
TABLE XVIII: MSP430F1121A PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.8 – 3.6 V</td>
</tr>
<tr>
<td>Active mode current</td>
<td>160 µA at 1 MHz, 2.2 V</td>
</tr>
<tr>
<td>Standby mode current</td>
<td>0.7 µA</td>
</tr>
<tr>
<td>Off mode current (RAM retention)</td>
<td>0.1 µA</td>
</tr>
<tr>
<td>Wake-up from standby mode time</td>
<td>&lt; 6 µs</td>
</tr>
<tr>
<td>Architecture</td>
<td>16-bit RISC</td>
</tr>
<tr>
<td>Instruction cycle time</td>
<td>125 ns</td>
</tr>
<tr>
<td>Flash memory</td>
<td>4 KB + 256 B</td>
</tr>
<tr>
<td>RAM</td>
<td>256 B</td>
</tr>
<tr>
<td>Timer</td>
<td>16-Bit</td>
</tr>
<tr>
<td>I/O pins</td>
<td>14</td>
</tr>
<tr>
<td>Presence of comparator for ADC</td>
<td>yes</td>
</tr>
<tr>
<td>Temperature</td>
<td>−40°C to 85°C</td>
</tr>
<tr>
<td>Price</td>
<td>3.40$</td>
</tr>
</tbody>
</table>

Peripherals are connected to the CPU using data, address, and control buses, so they can be easily accessed by general purpose commands. Finally, the instruction set consists of fifty-one instructions and any of those can independently operate over words or bytes.

All details related to the package and to the pins description are collected in Appendix D[17].

3.2.3  **MSP430F5438A**

Although the MSP430F1121A was the most addressed microcontroller in the older AraMiS applications, in this project the **MSP430F5438A** is going to be used since it is faster, it has larger memory capabilities and shows a greater number of GPIOs.
Figure 33: MSP430F1121A - functional block diagram[17]

Figure 34: Word formats and address within the MSP430 microcontroller[17][18]
Moreover, there were several compatibility issues between the MSP430F1121A and IAR, the most widespread environment for embedded systems programming. Those problems have been definitely solved with the new microcontroller, so the MSP430F5438A is supposed to be IAR compatible. Such a chip still belongs to the MSP430 family, so all benefits in terms of low power consumption, low cost and 16-bit RISC architecture are maintained. Additionally, as pointed out in Table XIX, the new microcontroller shows a wider connectivity and DMA capability to make faster data transfers with memory[18].
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.2 – 3.6 V</td>
</tr>
<tr>
<td>Active mode current (RAM execution)</td>
<td>140 µA at 8 MHz, 3 V</td>
</tr>
<tr>
<td>Active mode current (FLASH execution)</td>
<td>312 µA at 8 MHz, 3 V</td>
</tr>
<tr>
<td>Standby mode current</td>
<td>1.8 µA</td>
</tr>
<tr>
<td>Off mode current (RAM retention)</td>
<td>1.69 µA, 3 V</td>
</tr>
<tr>
<td>Wake-up from standby mode time</td>
<td>&lt; 5 µs</td>
</tr>
<tr>
<td>Architecture</td>
<td>16-bit RISC, up to 18 MHz</td>
</tr>
<tr>
<td>Flash memory</td>
<td>256 KB</td>
</tr>
<tr>
<td>SRAM</td>
<td>16 KB</td>
</tr>
<tr>
<td>Timer</td>
<td>3 units, 16-Bit</td>
</tr>
<tr>
<td>I/O pins</td>
<td>67</td>
</tr>
<tr>
<td>Presence of comparator for ADC</td>
<td>12-Bit, S/H</td>
</tr>
<tr>
<td>Connectivity</td>
<td>I²C, IrDA, LIN, SCI, SPI, UART/USART</td>
</tr>
<tr>
<td>DMA</td>
<td>Yes</td>
</tr>
<tr>
<td>Temperature</td>
<td>−40 °C to 85 °C</td>
</tr>
<tr>
<td>Price</td>
<td>3.73$</td>
</tr>
</tbody>
</table>

All details related to the package and to the pins description are collected in Appendix G[18].
3.2.4 Characterization in space conditions

There is not so much information concerning COTS components reliability in space applications because, generally, only space qualified devices are used in avionics. Despite that, a useful research has been carried out at the Surrey Space Centre (sponsored by ESA) for characterizing wireless COTS systems in space applications[6]. The systems which have been analyzed use three different SMT pairs of microcontrollers and transceivers: the MSP430 (with TX/RX CC2420, total mass equal to 23 g), the SoC (complete system on chip, total mass lower than 2 g) and the Atmega128 (with TX/RX CC1000, total mass equal to 18 g).

The first carried out test referred to vibration tolerance and the main objective was to verify whether the package could withstand the flight. Then it was expected to achieve the resonant frequency for each structure in order to identify the most dangerous vibration frequency. In this context, it is impossible to know a priori which vibrations are going to happen during the launch, so random vibrations in terms of amplitude and frequency must be considered. This random environment is specified in terms of acceleration power spectral density (PSD), over a frequency band ranging from 20 Hz to 2000 Hz (Figure 36, Figure 37 and Figure 38). In this context, the $g$ parameter is the gravitational acceleration, while the reference system is taken such that the $x/y$-axis identify the plane on which the integrated circuits are placed.

Experimental results pointed out that at low frequency (less than 200 Hz) there are no resonances for any system, so they are all suitable to be integrated in a launcher. When frequency increases, the SoC structure has two resonance points when vibrations are oriented along the z-axis (Figure 38). The conclusion is that both the Atmega128 and the MSP430 microcontroller
Figure 36: Vibration power spectral density over x-axis for different ICs[6]

Figure 37: Vibration power spectral density over y-axis for different ICs[6]
have packages which show good response to mechanical vibrations, while the use of SoC would require additional mechanical efforts to ensure its stability.

The second test took into account the thermal stress due to high temperature and huge heat variations. In an isolated thermal chamber, the temperature was made to vary from 80 °C to −40 °C according to the trend exposed in Figure 39.

After the first day, a sharp thermal excursion of 120 °C was emulated and both the minimum and the maximum temperatures were maintained for more than 20 hours. The result was that all devices continued to work properly and no package was damaged by thermal expansion.

Finally, a test referring to the total ionizing dose radiation was performed by increasing the dose level up to 30 Krad. During the process a set of parameters were recorded to analyze the quality of transmissions and the computing capability.
After 6 hours of monitoring, the MSP430 microcontroller resulted the best device since no anomalies arose. As a matter of fact, constant connectivity and no growth in the power consumption have been highlighted. In contrast, the SoC is the weakest component against
radiations since connectivity was completely lost just after 15 Krad, while Atmega128 remained in working condition with high power consumption due to latch-up.

### 3.3 Power Amplifier

The external power amplifier which is selected for the UHF channel is the RFMD RF6886. It is a suitable device because it provides an output level up to 37 dBm within 100 MHz and 1 GHz. The device is manufactured on the advanced InGaP HBT technology and has been designed for working as a final stage amplifier in the band of interest[21].

In order to achieve the required amplification and the 50 Ω impedance matching, the circuit shown in Figure 41 must be implemented.

<table>
<thead>
<tr>
<th>ID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>3 V - Voltage supply</td>
</tr>
<tr>
<td>$V_{reg1}$, $V_{reg2}$</td>
<td>2.8 V - Regulated supply to set driver/output stage DC bias</td>
</tr>
<tr>
<td>RF IN</td>
<td>RF input</td>
</tr>
<tr>
<td>RF OUT</td>
<td>RF output and bias for output stage</td>
</tr>
<tr>
<td>PIN4, PIN7-12, PIN20-21</td>
<td>No connect</td>
</tr>
</tbody>
</table>

According to the manufacturer’s specifications, key locations are red marked and the output ceramic capacitors (C17, C18 and C19) are all Johanson Hi-Q tight tolerance because they tend to exhibit very low DC leakage.
Figure 41: RF6886DS application circuit [21]
3.4 Power management

AraMiS architecture contains a suitable power bus in order to supply all electronic boards of the satellite. The required amount of energy is provided by rechargeable batteries able to get power from solar panels when they are exposed to the sunlight. The maximum available power is approximately 20 W, while the voltage varies between 12 V and 18 V.

The power amplifier which has been selected requires up to 3.1 A (peak current) and it needs a voltage supply equal to 3 V, so it is necessary to use a high-efficiency voltage regulator (buck switching converter). A suitable choice is given by the Texas Instruments TPS5450 step-down converter because it provides a wide input voltage range (from 5.5 V to 36 V) and up to 5 A continuous output current[19]. The design is carried out by means of the SwitcherPro Desktop tool, directly provided by Texas Instrument.

Both C1 and C2 are critical capacitors, so they must be substituted. As a matter of fact, the former is a tantalum capacitor, so the nominal DC voltage should be over-designed in order
### TABLE XXI: TPS5450 MANUFACTURER’S COMPONENTS DESCRIPTION

<table>
<thead>
<tr>
<th>ID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>330 µF (Tantalum) - 25 V - 3.5 A - Panasonic</td>
</tr>
<tr>
<td>C2</td>
<td>220 µF (Electrolytic) - 4 V - 40 mΩ ESR - 20% - Sanyo Electric</td>
</tr>
<tr>
<td>C3</td>
<td>10 nF - 20 V - 1%</td>
</tr>
<tr>
<td>C9</td>
<td>4.7 µF - 25 V - 20% - Murata Manufacturing</td>
</tr>
<tr>
<td>D1</td>
<td>Schottky diode - 50 V - 5 A</td>
</tr>
<tr>
<td>L1</td>
<td>18 µH - 5 A - 30 mΩ - CoilCraft</td>
</tr>
<tr>
<td>R1</td>
<td>10 KΩ - 100 mW - 1%</td>
</tr>
<tr>
<td>R2</td>
<td>6.81 KΩ - 100 mW - 1%</td>
</tr>
</tbody>
</table>

to avoid explosions. The latter is an electrolytic capacitor, so it is not feasible for vacuum applications. As a consequence, the input capacitors are changed with two 47 µF parallel ceramic capacitors and a 10 nF capacitor is added to delete high frequency noise. Regarding the output capacitor (C2), it is crucial to identify a suitable device having an equivalent series resistance as close as possible to 40 mΩ. In fact, higher values would lead to higher output voltage ripple, while too lower values would provide very small phase margin in the control loop. The selected capacitor is a 220 µF tantalum capacitor having 16 V over-designed DC voltage and 40 mΩ as ESR.

The following graph (Figure 43) points out that the efficiency related to the power regulator is approximately 80% in the mean operating region[19].

All details related to the functional diagrams and pin description of the buck converter are collected in Appendix F.
TABLE XXII: TPS5450 COMPONENTS REPLACEMENT

<table>
<thead>
<tr>
<th>ID</th>
<th>Replacement</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>C1a 47 µF - 25 V - 5 A - Murata</td>
</tr>
<tr>
<td>C1b</td>
<td>47 µF - 25 V - 5 A - Murata</td>
</tr>
<tr>
<td>C1c</td>
<td>10 nF - 50 V - 5 A - Panasonic</td>
</tr>
<tr>
<td>C2</td>
<td>220 µF (Tantalum)- 16 V - 40 mΩ ESR - Panasonic</td>
</tr>
</tbody>
</table>

Figure 43: Buck converter efficiency Vs Output current (Texas Instruments - SwitcherPro)

Since the power amplifier is the only high current-consumption component, for all the other electronic devices it is sufficient to use adjustable positive voltage regulators to achieve the required supply voltage (3.7 V ≤ V_{in} ≤ 38 V, 1.2 V ≤ V_{out} ≤ 32 V and I_{o} ≤ 100 mA)[20]. As a matter of fact, adjustable regulators do not require many passive components, so they ensure a greater board surface optimization with respect to switching converters. The drawback is the lower efficiency, but the current consumption is very low, so the power dissipation is negligible. In this specific case, a set of Texas Instruments LM317L is used to supply the microcontroller,
the transceiver, the oscillator, the power amplifier ($V_{reg1,2}$) and to provide the voltage reference for the temperature sensor.

In the foregoing schematic (Figure 44), $C_{in}$ allows to reduce the input noise coming from the power bus, while $C_o$ improves the transient response. The integrated circuit works to maintain a voltage reference over $R_1$ ($V_{ref} = 1.25$ V), then a voltage divider is implemented ($R_2$) to provide the required output voltage. The value of $R_2$ determines the output DC voltage according to the following equation:

$$V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 \ [V]$$

Since $I_{adj} \leq 100 \ \mu A$, it is possible to simplify the expression by neglecting the last term[20].

When external capacitors are used around any IC supplied by LM317L, it is necessary to add protection diodes (D1 and D2) in order to prevent that those capacitors discharge into the regulator. Due to the presence of many by-pass capacitors for the microcontroller, the equivalent
TABLE XXIII: DESIGN OF LINEAR REGULATORS WITH LM317L

<table>
<thead>
<tr>
<th>Application</th>
<th>$V_{required}$ [V]</th>
<th>$R_2$ [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC1020</td>
<td>3.3</td>
<td>402</td>
</tr>
<tr>
<td>MSP430</td>
<td>3.3</td>
<td>402</td>
</tr>
<tr>
<td>FOX924B</td>
<td>3.3</td>
<td>402</td>
</tr>
<tr>
<td>NTC thermistor</td>
<td>3.0</td>
<td>336</td>
</tr>
<tr>
<td>RF6886DS</td>
<td>2.8</td>
<td>300</td>
</tr>
</tbody>
</table>

Figure 45: LM317L Adjustable voltage regulator with protection circuit[20]

$C_o$ at the output of the regulator is large, so the protection diodes are required. The final circuit is shown in Figure 45.

Diode D1 prevents $C_o$ from discharging through the IC during a switch-off short circuit ($V_{in} = 0$), while diode D2 protects against capacitor $C_{adj}$ (when greater than 5 µF) from discharging through the IC during an output short circuit. Finally, LM317L is free from radiation related issues since it is completely based on BJT technology instead of CMOS.
3.5 Low-noise Amplifier

The CXE-2089Z integrated circuit properly works in the band of interest. It is based on the GaAs MESFET technology and provides a gain of 20.5 dB with a low noise figure equal to 1.5 dB. In order to ensure 50 Ω as both input and output impedance matching, the reference circuit shown in Figure 46 must be implemented[22].

![Figure 46: CXE-2089Z application circuit][22]

Since the objective is to integrate both the LNA and the transceiver over a unique PCB, the coaxial connectors (J1 and J2) are not going to be used. Such an amplifier is only shown as a possible choice for a future expansions because it is compatible in terms of sensitivity and
### TABLE XXIV: CXE-2089Z MANUFACTURER'S COMPONENTS DESCRIPTION

<table>
<thead>
<tr>
<th>ID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1, J2</td>
<td>Coax F - Trompeter Electronics SMA - Heilind Electronics</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>8 V - Voltage supply</td>
</tr>
<tr>
<td>L1</td>
<td>1 $\mu$H - CoilCraft</td>
</tr>
<tr>
<td>L2</td>
<td>10 nH - Toko America</td>
</tr>
<tr>
<td>C1</td>
<td>1 $\mu$F - Panasonic Industrial</td>
</tr>
<tr>
<td>C3, C4</td>
<td>10 nF DC blocking capacitors - Panasonic Industrial</td>
</tr>
<tr>
<td>C2</td>
<td>1200 pF - Panasonic Industrial</td>
</tr>
<tr>
<td>C6</td>
<td>1.8 pF - Taiyo Yuden</td>
</tr>
<tr>
<td>PIN1</td>
<td>RF Input pin</td>
</tr>
<tr>
<td>PIN2, PIN4</td>
<td>GND</td>
</tr>
<tr>
<td>PIN3</td>
<td>RF Output and DC bias pin</td>
</tr>
</tbody>
</table>

output power to the transceiver side. Anyway, it will not be adopted in the project because the AraMiS specifications are already met.

#### 3.6 Protection Circuits

The two destructive phenomena which may appear during the satellite lifetime are basically the *latch-up* and the *electrostatic discharge* (ESD). The 1B127 hybrid circuit developed by *Neohm* is a suitable latch-up countermeasure because it has been designed for LEO satellites and the input voltage is supposed to range from 3 V to 18 V, exactly matching the AraMiS power bus. Since the power amplifier does not contain CMOS devices, such a protection circuit is only used to preserve the microcontroller and the transceiver.

The circuit acts as a differential switch between the power bus and the telecommunication tile intended as a general load (Figure 47). The current flowing into the circuit is sensed by means of a differential amplifier over the resistor $R_S$, then, if the voltage drop becomes
greater than the reference (i.e. a latch-up condition occurs), the monostable circuit opens the power switch. Finally, once the circuit has been opened with the consequent prevention of any damage (turn-off time lower than 100 µs), the current drops, so the switch is again closed (recovery time is approximately equal to 10 ms). According to the datasheet specifications

\[ R_S = \frac{V_{th}}{I} \]

where \( V_{th} \) is the threshold voltage of the power switch (30 mV), while \( I \) is the maximum allowed current. In the specific case, according to the maximum current required by both the transceiver and the microcontroller, the maximum tolerated current is assumed equal to 100 mA, so \( R_S = 0.3 \, \Omega \). Moreover, \( R_S \) must be properly sized to support 3 mW power, since in the worst case \( P = \frac{V_{th}^2}{R_S} = \frac{(100 \, \text{mV})^2}{0.3 \, \Omega} \). In order to provide a safe current return path whenever the switch is open, LSC is directly connected to the active current node. As a result, if the circuit is working, LSC pin is not connected to ground because the switch is open, while, in case the the SEU occurs, the power switch opens and the current flows to GND.
On the other hand, the electrostatic discharge can occur whenever padstacks are recklessly touched or when they transit through regions carrying high electric fields. If sparks arise, huge voltage drops ($\sim$ KV) take place and destructive alterations such as either dielectric or junction breakdown could happen. Generally, all I/O pins in the integrated circuits are protected by clamping circuits like the one shown in Figure 48.

Whenever a negative peak strikes the I/O pin, D2 becomes a short circuit, so the spark is discharged to ground. In contrast, if a highly positive peak occurs, both D1 (direct) and D3 (breakdown) conduct, then the spark is again discharged to ground preserving both the integrated circuit and the voltage supply.

### 3.7 Load switch

According to UML specifications, the OBC must have the capability to attach/detach the telecommunication module through the corresponding interface, while the microcontroller must
attach/detach the power amplification chain. Those operations are accomplished by driving the enable pin (EN) of the schematic in Figure 49, since it handles a high-side switch.

The power MOS $\text{IRLM6402}$ is a suitable transistor for this application because it is a p-channel transistor and it supports a DC drain current up to $3.7 \text{ A}$ (greater than the overall average amount required by the board). Additionally, the second transistor is the n-channel MOS $\text{NTA7002NT1G}$ and it has a threshold voltage lower than $1.5 \text{ V}$, then it can be driven by the EN digital signal coming from the OBC.

### 3.8 Sensors

In order to provide all the housekeeping data related to the satellite and all its subsystems, a set of standard sensors must be included in the board. Basically, the mission controller wishes to monitor both electrical parameters and temperature because they are directly associated to
Figure 50: 20 V voltage sensor (Mentor Graphics environment)

the safe operating region of any electronic unit. All sensors are analog and take advantage of the analog-to-digital converters embedded in the microcontroller for providing numerical data. Since the 12-bit ADCs are all integrated in the CPU, just simple routines are used to program the sampling frequency. The decoding function must consider that the ADC dynamic range is 2.5 V, so suitable conditioning circuits may be required.

The voltage supplied by the power distribution bus is measured through the following voltage sensor. It is a voltage divider with high input impedance to avoid electrical variations in the main circuit and reduce power consumption as much as possible. Moreover, there is also a capacitor to ensure the holding time for the ADC and to cut off quick voltage variations (Figure 50).
Additional four 5 V-voltage sensors are also used to measure all the adjusted voltages and the output associated to the DC-DC power converter.

For both the voltage sensors, \( V_{\text{measured}} = \frac{D \cdot FS}{k \cdot 2^b} \), where \( D \) is the digital number acquired by the microcontroller, \( FS \) is the sensor dynamic range, \( k \) is the factor associated the specific sensor and \( b \) is the number of available bits. In this case, \( k \) is equal to 0.1277 for the 20 V-sensor, while it is 0.5 for the other one.

Secondly, the current supplied by the power distribution bus is measured through a current sensor. That is based on the INA138 integrated circuit provided by Texas Instruments and a single capacitor is again added to provide holding time and low-pass filtering capability for the ADC.
The transresistance gain of the circuit is $V_o = I_S \frac{R_S \cdot R_L}{5 \cdot K_T}$, where $I_S$ is the current to be measured. The device converts the differential input voltage over $R_S$ to a current output, then this current signal is converted back to a voltage through the external load resistor $R_L$. In order to achieve high accuracy and get a measurement range of about 5.5 A (5.682 A nominal, greater than the maximum needed current), a 22 mΩ resistor is used as $R_S$. That is because in this way the maximum output voltage is 2.5 V and such a value fully matches the ADC input dynamic range.

Temperature monitoring is based on a NTC thermistor ranging from $-40^\circ$C to $150^\circ$C with a thermal constant equal to 8 s. The circuit acts as a voltage divider with high input impedance, then the output voltage depends on the resistance associated to the NTC, that is a function of temperature. A final remark concerns its position because the temperature which is going to
be measured will depend on the specific placement of the sensor. Since the most critical part of
the circuit is the power amplifier (regarding the thermal dissipation), the sensor must be placed
as close as possible to that unit.
Figure 54: Temperature sensor (Mentor Graphics environment)

Figure 55: NTC - Transfer function (MATLAB)
3.9 External interfaces

According to UML specifications related to the AraMiS system, the radio frequency module has three specific wired connections to the external world.

Firstly, a 14 pins JTAG connector is used to both externally program and debug the microcontroller. As a matter of fact, the IAR Embedded workbench is compatible with Ti-USB FET debugger and that is the standard provided by Texas Instrument to interface a PC with the MSP430.

The following list provides the JTAG pin description.

- TCK is used to load the test mode data from the TMS pin and the test data on the TDI pin. On the falling edge, output data is sent on the TDO pin. This line needs to be
TABLE XXV: PIN DESCRIPTION OF THE JTAG CONNECTOR

<table>
<thead>
<tr>
<th>PIN</th>
<th>ID</th>
<th>NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TDO</td>
<td>Test Data Output</td>
</tr>
<tr>
<td>2</td>
<td>PWR_IN</td>
<td>Power Input</td>
</tr>
<tr>
<td>3</td>
<td>TDI</td>
<td>Test Data Input</td>
</tr>
<tr>
<td>4</td>
<td>PWR_OUT</td>
<td>Power Output</td>
</tr>
<tr>
<td>5</td>
<td>TMS</td>
<td>Test Mode Select</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>7</td>
<td>TCK</td>
<td>Test Clock</td>
</tr>
<tr>
<td>8</td>
<td>TST</td>
<td>Test Set</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>11</td>
<td>RST</td>
<td>Reset</td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>No connection</td>
</tr>
</tbody>
</table>

terminated in order to reduce reflections and the termination should be a 68 Ω resistor in series with a 100 pF capacitor to ground.

- **TMS** controls the operation of the test logic by receiving the incoming data. The line should have a 10 KΩ pull-up resistor.

- **TDI** receives serial input data. The line should have a 10 KΩ pull-up resistor.

- **TDO** outputs serial data which comes from either the test data registers or instruction registers. The line should have both a 10 KΩ pull-up resistor and a 22 Ω series resistor placed near the device in the JTAG chain.

- **RST** will asynchronously reset the JTAG test logic regardless of the state of TMS or TCLK.
• *PWR_IN* and *PWR_OUT* can be used to provide/sense a stable voltage equal to 3.3 V.

• *TST* sets the JTAG test mode on the microcontroller.

Beyond test purposes and the initial programming phases, the board will exclusively communicate to the OBC by means of the *SPI interface* and the 6 *backdoor pins*.

![Figure 57: SPI interface](image)

The 6 backdoor pins previously introduced are used for remote controlling the OBC by the ground segment. In fact, those pins are directly connected to the *FPGA* inside the AraMiS core and they allow to modify portions of the programmable digital hardware.

However, the great majority of information and commands will transit through the 4-wires SPI interface, so that represents the main connection between the telecommunication tile and the on-board computer. In Figure 57, a typical master-to-slave configuration is shown and that represents the actual configuration between the microcontroller (master) and the transceiver (slave).
TABLE XXVI: SIGNALS DESCRIPTION OF THE SPI INTERFACE

<table>
<thead>
<tr>
<th>ID</th>
<th>NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>MOSI</td>
<td>Master Output/Slave Input</td>
</tr>
<tr>
<td>MISO</td>
<td>Master Input/Slave Output</td>
</tr>
<tr>
<td>SS</td>
<td>Slave Select</td>
</tr>
</tbody>
</table>

In order to begin the communication, the master firstly configures the clock using a frequency less than/equal to the maximum frequency that the slave device can support. Then, the master transmits a 0-logic signal as a chip select bit (SS) for the desired slave. During each SPI clock cycle, a full duplex data transmission occurs since the master sends a bit on the MOSI line and reads from MISO line, while the slave operates in the complementary way. Transmissions normally involve two shift registers (one in the master and the other in the slave) connected in a ring: data is usually shifted out with the most significant bit first, while getting a new least significant bit into the same register. After that a register has been shifted out, the master and slave have exchanged register values, then each device takes that value and writes it to memory. If there is more data to exchange, the shift registers are loaded with new data and the process repeats.

The physical interface between the UHF board and the OBC must be suitable for SPI communication, backdoor pins and power supply. The set of all the available pins is grouped in the *J6-connector* and that is depicted in Table XXVII.
### TABLE XXVI: PIN DESCRIPTION OF THE J6-INTERFACE (J2 CONNECTOR)

<table>
<thead>
<tr>
<th>PIN</th>
<th>ID</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BACKDOOR_INT</td>
<td>Backdoor signal reset</td>
</tr>
<tr>
<td>2</td>
<td>BACKDOOR_0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>BACKDOOR_1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>BACKDOOR_2</td>
<td>6-pin for the backdoor interface</td>
</tr>
<tr>
<td>5</td>
<td>BACKDOOR_3</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>BACKDOOR_4</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>BACKDOOR_5</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>RF_POWER</td>
<td>Power Distribution Bus (12 – 18 V)</td>
</tr>
<tr>
<td>9</td>
<td>RF_POWER</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>RF_AN0</td>
<td>Analog signal (not used)</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>12</td>
<td>RF_AN1</td>
<td>Analog signal (not used)</td>
</tr>
<tr>
<td>13</td>
<td>CS5</td>
<td>SPI - SS</td>
</tr>
<tr>
<td>14</td>
<td>OBC_HZ_IN</td>
<td>High Impedance</td>
</tr>
<tr>
<td>15</td>
<td>TX5/MOSI_FPS</td>
<td>SPI - MOSI</td>
</tr>
<tr>
<td>16</td>
<td>OBC_HZ_OUT</td>
<td>High Impedance</td>
</tr>
<tr>
<td>17</td>
<td>RX/MISO_FPS</td>
<td>SPI - MISO</td>
</tr>
<tr>
<td>18</td>
<td>SCKS</td>
<td>SPI - SCLK</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>Analog ground</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>Digital ground</td>
</tr>
</tbody>
</table>

The presence of two wires for the power distribution bus allows to achieve twice as much current. In this way, the maximum DC current which can flow through the board is 3.5 A and such a value fully matches the overall need.
CHAPTER 4

UNIFIED MODELING LANGUAGE

As mentioned in the thesis introduction, ensuring a high level of integration among different developers is a crucial point in any complex design. As a matter of fact, it is important to share specifications and check the system constraints in order to avoid incompatibility issues and make any design reusable. In this thesis, the entire documentation associated to the telecommunication tile (e.g. parts, schematics, electrical details and use cases) must be provided and such a task is performed by means of the UML description. In this chapter, the UML environment is briefly introduced, then the system description is carried out.

4.1 General description

UML (Unified Modeling Language) is a visual language which allows to depict complex architectures composed by subsystems of different nature, such as electronic circuits, software algorithms, mechanical structures, business models and so on. By means of both diagrams and relationships, several projects can be integrated, so that documentation, features and specifications are easily shared among the designers. That approach also leads to an effective work subdivision, then each specific module/task can be independently assigned without losing the overall view. In this thesis, Visual Paradigm Standard Edition is going to be used for UML descriptions (use case diagrams, class diagrams and sequence diagrams) and for the automatic generation of C-language code.
Firstly, use case diagrams highlight what the system must do and all the interactions with the external world. In this context, users and subsystems connected with the RF module from outside are called *actors*, while the *use cases* specify the available actions and how objectives are achieved. In the following example (Figure 58), the on-board computer (OBC) must manage the set of operations (use cases) shown in the ellipses.

![Use Case Diagram](image-url)

*Figure 58: Example of use case diagram (Visual Paradigm)*

Use cases can be interconnected as either *inclusion* or *extension* and both relationships are identified by means of dashed arrows. In case of inclusion, the base use case includes the actions expressed by the other one. For instance, in the foregoing picture (Figure 58) the “receive” use
case intrinsically includes a “packet available”. On the other hand, the extension relationship provides an optional behaviour which can be adopted by the base use case.

Secondly, class diagrams show the general structure of the objects according to their own services and their relationships with the other entities. Each element is defined by its name and it is graphically associated to a rectangular box. Each box contains both attributes (constants, variables) and methods (functions, routines), similarly to any other programmable object in JAVA or C++. Attributes can be of several types, ranging from the standard ones (char, float, integer) to the customize structures, while methods can receive parameters and return values like C-functions. Classes are related to each other in order to exchange information and all the associations are pictorially represented by means of several kind of arrows. Those arrows can identify aggregation (whole-part relationship without a strong life-cycle dependency on the container), composition (whole-part relationship with a strict life-cycle dependency), generalization (superclass-subclass relationship), containment (content-container relationship), association (not well defined relationship), self-dependence, and so on. Their direction identifies the master for each relationship (not necessarily the information flow) and the chain of all messages exchanged by the objects allows to accomplish a specific use case. In order to group together different classes which belong to the same area, it is possible to define stereotypes. In this project they are used to identify electronic modules (yellow), electronic components (orange), materials (violet) and software classes (green).
Finally, sequence diagrams show different processes that live simultaneously (very often as a causal relationship) and the corresponding messages which are exchanged. There are parallel vertical time-lines (*lifelines*) and horizontal arrows which identify the links among processes. Such a structure allows to graphically describe both SW routines and complex scenarios (Figure 60).

Figure 59: Example of class diagram (Visual Paradigm)
4.2 Use case diagrams

The project is organized in three use-case diagrams which respectively describe the TX/RX operations, the housekeeping functions and the interactions between the RF module and the OBC.
Figure 61: BkIB31 TX/RX - Use case diagram (Visual Paradigm)
Figure 62: Bk1B31 Housekeeping - Use case diagram (Visual Paradigm)
Figure 63: Bk1B31 Housekeeping - Use case diagram (Visual Paradigm)
The following list shows the documentation associated to the main actors and use cases.

- **OBC - actor**: the On Board Computer or any other processing unit willing to communicate via a RF channel.

- **Tile Processor - actor**: the processor hosted on each tile, which is in charge of handling all Tile functions and subsystems.

- **Configurator - actor**: the person in charge of configuring HW/SW parameters according to spacecraft architecture and mission requirements.

- **Transmit - use case**: sends the content of the first data buffer to be sent (plus header/footer) to ground and: generates data header (including synchronization, length and CRC), modulates, encodes. Does not handle: packet numbering, retransmission request, ACK/NACK of packet reception. When the System is in Standby mode, the RF transmitter is disabled and cannot therefore transmit any signal to ground.

- **Receive - use case**: receives up to 256 B of data (plus header/footer) from ground and: demodulates, decodes, synchronizes on bit, byte and packet start and end, stores packet into a buffer, checks length and CRC. Does not handle: packet numbering, retransmission request, ACK/NACK of packet reception. When a packet has been received and the CRC is correct, it signals to the Packet Available use case. When the System is in Standby mode, the RF receiver is disabled and cannot therefore receive any signal from ground.
- **Packet composition - use case**: builds the packet to be sent according to the AX.25 protocol. Starting from the payload, header and footer are inserted to generate the final packet. The CRC use case is called to retrieve the CRC sequence.

- **Packet available - use case**: tells if a packet (received from ground) is available in the buffer. The corresponding flag is raised as soon as a new packet is received (after the reading it is lowered). The CRC code is retrieved to know if the packet is corrupted. If the CRC is correct, payload can be sent to the j6 Connector through either the SPI-interface or the backdoor pins.

- **CRC - use case**: computes the CRC for the bit-sequence received as an input.

- **Write data - use case**: stores up to 256 B of data in the first available buffer.

- **Read data - use case**: reads data from the first received data buffer. If not data is available, the result is unpredictable. The OBC shall either read data upon receiving the Data Received flag or call the Data Available use case.

- **SendToOBC - use case**: the payload is sent to the OBC through the SPI-interface.

- **Backdoor - use case**: the payload is sent to the backdoor-interface for directly controlling the on-board FPGA.

- **Configure 1B31 - use case**: configures the following 1B31 module parameters: bit rate, output power, channel, FSK/GFSK modulation.

- **Store Program - use case**: loads a SW architecture inside the microcontroller memory in order to manage/use/test the 1B31 On-Board Radio Frequency Module.
- **Standby - use case**: puts the system into a standby mode where: internal processor is in sleep mode but is able to listen to the bus, housekeeping sensors are either disabled or unpowered, RF receiver is either disabled or unpowered. When in Standby mode, the System can wake up if any command comes from the OBC. It uses the Module Standby use case of 1B45 package. After a given timeout, the system automatically calls the Module Wake Up use case (e.g. for safety).

- **Wakeup - use case**: wakes up the internal processor and exits the standby mode where: internal processor runs normally, housekeeping sensors are enabled, RF RX/TX hardware is enabled. It uses the Module Wakeup use case of 1B45 package.

- **Get PA Current - use case**: provides the main current consumption of the board. Bk1B132F-Current-Sensor is located at the output of BklB121D-Load-Switch-High-Voltage, so current is sensed only if BklB31A1-Transceiver-437MHz attached. The current consumption associated to Bk1B131C-Voltage-Sensor, Bk1B133B-Temperature-Sensor, Bk1B31A1-Reg3V-437MHz and Bk1B131A-Voltage-Sensor (the one for the voltage measurement associated to the output of Bk1B31A1-Reg3V-437MHz) is not measured. Although the current consumption of all the other electronic modules is in principle sensed, the current measurement basically corresponds to the feeding of the power amplifier. As a matter of fact its contribution is the great majority (two orders of magnitude) when compared to the other sensors, the linear regulators and both the transceiver and the processor tile. The current range is $0 - 5.682$ A. $I_{\text{measured}} = D \cdot k$, where D is the output of the ADC and $k = 3.15$ mA.
• *Get PA Current - use case*: provides the temperature associated to the power amplifier integrated circuit. The temperature sensor is located within 1 cm far from the amplifier. In order to get the temperature, Bk1B31A1-OBRF-437MHz must be attached. \( T_{\text{measured}} = f^{-1}(D \cdot k) \), where D is the output of the ADC and \( f^{-1} \) is the inverse function associated to the temperature sensor Bk1B133B-Temperature-Sensor. \( k = 600 \mu \text{V} \).

• *Get Voltages - use case*: provides up to 5 supply voltages.

• *Get 3 V power voltage - use case*: gets the input voltage just at the output of the Power Switching. The voltage range is 0 – 5 V. \( V_{\text{measured}} = D \cdot k \), where D is the output of the ADC and \( k = 2.44 \text{ mV} \). In order to get the voltage, Bk1B31A1-OBRF-437MHz must be attached.

• *Get PDB Voltage*: measures and returns the input PDB voltage just at the output of Bk1B121D-Load-Switch-High-Voltage with a signed 16-bits integer. \( V_{\text{measured}} = D \cdot k \), where D is the output of the ADC and \( k = 38.2 \text{ mV} \). In order to get the voltage, Bk1B31A1-OBRF-437MHz must be attached. It returns housekeeping data (voltage) using the Get Module Housekeeping use case of 1B45 package, in the Housekeeping[GET-PDB-VOLTAGE] variable.

• *Get Reg-3V0*: gets the input voltage just at the output of Bk1B31A1-Reg3V-437MHz. The voltage range is 0 – 5 V. \( V_{\text{measured}} = D \cdot k \), where D is the output of the ADC and \( k = 2.44 \text{ mV} \). In order to get the voltage, Bk1B31A1-OBRF-437MHz must be attached.
• **Get Reg-2V8**: gets the input voltage just at the output of Bk1B31A1-Reg2V8-437MHz. The voltage range is 0 – 5 V. \( V_{\text{measured}} = D \cdot k \), where D is the output of the ADC and \( k = 2.44 \text{ mV} \). In order to get the voltage, Bk1B31A1-OBRF-437MHz must be attached.

• **Get Reg-3V3**: gets the input voltage just at the output of Bk1B31A1-Reg3V3-437MHz. The voltage range is 0 – 5 V. \( V_{\text{measured}} = D \cdot k \), where D is the output of the ADC and \( k = 2.44 \text{ mV} \). In order to get the voltage, Bk1B31A1-OBRF-437MHz must be attached.

• **Choose Channel**: chooses channel among four predefined frequencies defined at compile-time via Set Frequencies use case. By default, first frequency is chosen at boot.

• **Set Transmission Power**: Selects among different power levels. After one day (approx) it automatically resets to the highest power level.

• **Enable PA**: physically connects the power supply for the PA unit through the Bk1B121D-Load-Switch-High-Voltage.

• **Disable PA**: physically disconnects the power supply for the PA unit through the Bk1B121D-Load-Switch-High-Voltage.

• **Get Latchup Number**: gets the number of latch-up events which occurred.

• **isolateRF**: isolates the RF module by opening an external switch.

• **Set Frequencies**: configures at compile-time the frequencies of up to four channels associated with the satellite. The channels shall be in the same band according to the PLL design.
• Module Housekeeping: an autonomous function which periodically samples (with period SAMPLETIME), calibrates and stores a number of (model element not found)-defined housekeeping data. Values are stored as either short or ushort words, with (model element not found)-defined resolution (at most 16 bits), in the housekeeping : short[LENGTH-HOUSEKEEPING] vector. The (model element not found) shall define a list of parameters to be acquired containing at least, for each parameter: type of parameter and location of sensor resolution (number of bits and signed/unsigned data type) scale factor (namely, number of physical units per each unit of stored parameter) offset (namely, real value corresponding to a stored 0 value) sample rate (samples/s) and optional analog/digital filtering index of data into the internal housekeeping : short[LENGTH-HOUSEKEEPING] vector (starting from 0). The length of housekeeping : short[LENGTH-HOUSEKEEPING] vector shall be at most 128 short. This function also optionally optional optional computes statistics (min, max and average values) of a subset of housekeeping : short[LENGTH-HOUSEKEEPING] vector; namely, LENGTH-STATISTICS elements starting from index FIRST-STATISTICS. The Get Module Housekeeping use case returns the last acquired housekeeping : short[LENGTH-HOUSEKEEPING] vector. The Get Module Housekeeping History use case returns history of the last DEPTH-HISTORY samples of the housekeeping : short[LENGTH-HOUSEKEEPING] vector (or a part of it, namely LENGTH-HISTORY elements starting from FIRST-HISTORY), for at most 256 B of data.
4.3 Class diagrams

Figure 64: System description - Overall view - class diagram (Visual Paradigm)
Figure 65: System description - Region A - class diagram (Visual Paradigm)
Figure 66: System description - Region B - class diagram (Visual Paradigm)
Figure 67: System description - Region C - class diagram (Visual Paradigm)
Figure 68: System description - Region D - class diagram (Visual Paradigm)
Figure 69: System description - Region E - class diagram (Visual Paradigm)
Figure 70: System description - Region F - class diagram (Visual Paradigm)
Figure 71: System description - Region G - class diagram (Visual Paradigm)
Figure 72: System description - Region H - class diagram (Visual Paradigm)
Figure 73: System description - Region I - class diagram (Visual Paradigm)
Figure 74: System description - Region L - class diagram (Visual Paradigm)
4.4 Sequence diagrams

Two sequence diagrams have been selected and analyzed as an archetype, while all the other ones are collected in Appendix I.
In order to enable the RF module, the system must show the following interactions in this order:

- the power supply provided by the power distribution bus (12-18 V) must be connected to the J6-interface (RF-POWER);
- power supply feeds the load switch through the interface (IN);
- OBC enables the RF module by closing the load switch (OBC-HZ-OUT);
- the load switch is closed, so that the board is fed by the power distribution bus (EN).
Figure 77: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
In order to get the output voltage of the buck converter, the system must show the following
interactions in this order:

- the power supply provided by the power distribution bus (12-18 V) must be connected to
  the J6-interface (RF-POWER);
- power supply feeds the load switch through the interface (IN);
- OBC enables the RF module by closing the load switch (OBC-HZ-OUT);
- the load switch is closed, so that the board is fed by the power distribution bus (EN);
- since the load-switch is closed, power supply feeds the other load switch (IN);
- the load switch is closed, so that the power supply feeds the voltage regulator (EN);
- since the load-switch is closed, power supply feeds the DC-DC buck converter (DCin);
- the voltage is detected by the sensor;
- the voltage is sensed by the voltage sensor. The wire carrying this analog signal is con-
  nected to the on-board computer (IN);
- the analog signal is converted to a digital one. Then, the corresponding number is multi-
  plied by a suitable conversion-constant to achieve the real value associated to the measured
  voltage ();
- the digital value is stored in the housekeeping vector according to the sampling time
  (acquire);
- the housekeeping vector is read by the OBC (getHousekeeping).
CHAPTER 5

COMMUNICATION PROTOCOL

The telecommunication subsystem intrinsically requires a communication protocol in order to provide a reliable communication channel between the satellite and the ground station. Since AraMiS is going to work in the radio amateur framework, the associated radio amateur standard (i.e., Packet Radio) is going to be adopted. In this chapter, the frame description is pointed out since it is necessary at software level design, then a deep analysis on the CRC computation is carried out. In the end, the hardware implementation is shown, while the software CRC algorithm will be presented in chapter associated to the SW architecture.

5.1 Packet radio

Packet radio is one of the major digital radio communication modes and it is a form of packet switching technology used to transmit digital data via wireless channels. By the early 1990s, packet radio was not only intended as a way to send textual information, but also to transmit generic files, handle repetitive communications and control remote systems.

In Montreal, radio amateur operators began to use packet radio in 1978, when the first ASCII encoded data was successfully transmitted over VHF radio amateur frequencies by means of home-built equipment. In few years standardized equipment (TNC) started to be produced and packet radio became popular in North America. As a consequence, many services such as
taxis, tow trucks and police adopted packet radio for providing simple mobile data transmission systems.

Nowadays, packet radio is used in the radio amateur framework to build up wireless computer networks and, since AraMiS transmissions take place within the radio amateur frequency range, that standard is going to be adopted.

According to the OSI model (Figure 78), packet radio networks can be described in terms of physical, data link, and network layer protocols:

- the physical layer consists of a modem and the radio channel;

- the data link layer protocol is AX.25;

- the network layer is mostly undefined since packet radio was mainly intended for point-to-point links (e.g. AraMiS). However, in to provide automatic data routing among several stations, a set of compatible network protocols have been developed (e.g. NET/ROM & TheNET, ROSE, FlexNet and TexNet).

5.2 AX.25

Packet radio networks use AX.25 as a data link layer protocol, that is derived from the more general X.25 suite and adapted for radio amateur use. AX.25 is a pre-OSI model protocol, so at the origin the layering was not clearly delineated. Consequently, it does not define only the data link layer, but also the physical one in the OSI stack. However, since both the transceiver and the UHF channel have been already identified, the goal is to use AX.25 just for the data link layer specifications.
In this context, packet radio transmissions are based on small blocks of data (frames) of three different types:

- **information frame (I frame)**;
- **supervisory frame (S frame)**;
- **unnumbered frame (U frame)**.

Each frame is composed of several *fields* which are shown in Figure 79 and described in the following.

- The *Flag Field* is one byte long (01111110₂ or 7E₁₆) and it is required to distinguish both the beginning and the end of each frame. Two adjacent frames may share one flag, which would denote the end of the first frame and the beginning of the next one. As a result of...
The *bit stuffing* procedure, this sequence does not occur anywhere else inside the frame. Moreover, flags are continuously sent to denote the *idle state* when no packets are sent.

- The *Address Field* is necessary to identify both the frame source and its destination. Optionally, it also consists of two additional sub-fields for the amateur callsign and the SSID. The former is made up of upper-case alphanumeric ASCII characters, while the SSID is a four-bit integer that uniquely identifies multiple stations within the same call-sign. Basically, SSID performs the same function of the ports in the TCP architecture.

- The *Control Field* is used to identify the type of the incoming frame and it also allows to monitor several attributes associated to the connection. Such a field can be one or two bytes long and may use sequence numbers to maintain the data exchange integrity.

- The *PID Field* is optional and allows to identify which kind of network layer protocol is present.

- The *Info Field* is associated to the information payload.

---

**Figure 79: AX.25 frame composition[3]**

<table>
<thead>
<tr>
<th>Flag</th>
<th>Address</th>
<th>Control</th>
<th>PID</th>
<th>Info</th>
<th>FCS</th>
<th>Flag</th>
</tr>
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<tr>
<td>01111110</td>
<td>112/224 Bits</td>
<td>8/16 Bits</td>
<td>8 Bits</td>
<td>N*8 Bits</td>
<td>16 Bits</td>
<td>01111110</td>
</tr>
</tbody>
</table>

**U/S - frame**

<table>
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<tr>
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<th>PID</th>
<th>Info</th>
<th>FCS</th>
<th>Flag</th>
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</thead>
<tbody>
<tr>
<td>01111110</td>
<td>112/224 Bits</td>
<td>8/16 Bits</td>
<td>8 Bits</td>
<td>N*8 Bits</td>
<td>16 Bits</td>
<td>01111110</td>
</tr>
</tbody>
</table>

**I - frame**
The FCS Field contains a sixteen-bit number computed by the sender over the Address, Control, and Information fields of the frame. This specific field provides a method which allows the receiver to detect errors that may have been occurred during the transmission.

In order to achieve more details related to the frame structure, refer to Appendix E.

5.3 Cyclic Redundancy Check

The most popular FCS algorithm is the CRC. It is an error-detecting code commonly used in digital networks and storage devices to detect accidental data changes. Once the data frame is generated, a polynomial division between the packet content and a generator string is performed. Then, a check value based on the remainder of such a division is attached. The receiver computes the calculation again, then data corruption is highlighted whether the check values do not match.

Calling $i(x)$ the information polynomial, $g(x)$ the divider (i.e. the generator polynomial), $q(x)$ the quotient polynomial, $r(x)$ the remainder, $n$ the degree of final codeword to be transmitted and $k$ the $i(x)$ degree, the following relation holds:

$$x^{n-k}i(x) = q(x) \cdot g(x) + r(x)$$

The transmitted codeword is going to be $b(x) = i(x) \& r(x) = x^{n-k}i(x) + r(x)$, where “$\&$” is the concatenation operator and $r(x)$ is the remainder of the division between $x^{n-k}i(x)$ and $g(x)$.

The receiver can compute the same division because the generator is shared at design level. The result is going to be:

$$\frac{b(x)}{g(x)} = \frac{x^{n-k}i(x)+r(x)}{g(x)} = \frac{q(x) \cdot g(x)+r(x)+r(x)}{g(x)}$$
Since all the operations belong to the *Galois space*, there is no difference between bitwise sum or difference, so \( r(x) + r(x) = r(x) - r(x) = 0 \) and \( \frac{b(x)}{g(x)} = q(x) \). Hence, if no errors occur the receiver does not get any remainder from the division. Otherwise, the actual received codeword would be \( b'(x) = b(x) + e(x) \), where \( e(x) \) is a fictional polynomial associated to the occurred errors. In this situation the remainder would be \( \frac{e(x)}{g(x)} \neq 0 \).

In Figure 81, an example shows how the CRC application works.

The crucial point is the choice of \( g(x) \) because it determines the error detection capability.
A single bit error in position $i$-th can be detected only if $g(x)$ has more than one term. That is because such an error is associated to $e(x) = x^i$, then if $g(x)$ contains multiple terms, $\frac{x^i}{1+x^i}$ produces a non-zero remainder.

- Double bit errors can be detected if $g(x)$ is irreducible. That is because, whenever $g(x)$ cannot be factorized, $\frac{x^i+x^j}{g(x)} = \frac{x^i(1+x^{j-i})}{g(x)}$ produces a non-zero remainder.

- Odd numbers of bit errors can be detected if $g(x)$ has $(x+1)$ as a factor.

Since the last two conditions are conflicting, but the channel is not supposed to be very much noisy, only the first two points are considered at the same time.

Regarding the CRC implementation, the algorithm can be normally executed in software, but there is also an effective hardware structure based on LFSR which easily computes the remainder when the generator is a primitive polynomial. The circuit implementation is derived from the Fibonacci (or many-to-1) schematic and it is depicted in Figure 82.
Given any primitive polynomial in the form $x^k + \ldots + 1$, there are four rules to design the corresponding digital circuit for computing the remainder:

- when $x^k = 1$, the $FF_0$ output is directly connected back to the D input of $FF_{k-1}$;
- $x^0$ is always ignored;
- each term in the $x^i$ form leads to an XOR connection between $FF_{k-i-1}$ and $FF_{k-i}$;
- an additional XOR gate is required at the input of the digital machine.

In case of $g(x) = x^4 + x + 1$, the digital HW implementation is shown in Figure 83.

Now, the entire process to achieve the reminder is shown in case of a different generator polynomial (Figure 84).

The input codeword bitwise circulates in the circuit until all bits are entered, then the register contains the remainder of the division. Since the AraMIS architecture does not contain any specific HW module for the CRC implementation, a set of suitable SW algorithms is going to be provided in the following chapter.
4-bit example, uses $x^4 + x^3 + 1$
- $x^3 \iff$ xor between FF1 and FF0

$$g(x) = x^4 + x + 1$$

Message sent:

1 0 1 1 0 0 1 1 0 1 0

- When MSB is 0, just shift left, bringing in next bit
- When MSB is 1, XOR with divisor and shift left

Figure 83: Example of 4-bit HW remainder generation for CRC application

Figure 84: Entire CRC-code generation process
5.4 High Level Data-Link Control

HDLC defines a protocol which can be located within the OSI stack just between AX.25 and the physical layer[3]. In the AraMiS background, HDLC defines a line encoding which alters the data stream in order to improve transmission performance. It basically provides three functions:

- **NRZI encoding**;
- **bit stuffing**;
- **frame delimiting**.

NRZI encoding (Figure 85) provides differential encoding for the bit stream to be transmitted. That works by encoding data according to the difference between adjacent bits. In fact, a 0-logic corresponds to a change in the output logic level, while 1-logic is associated to a no change in the output.

Regarding this, the absolute value of the output is irrelevant because only the changes in the encoded digital signal are meaningful, hence the two possible output waveforms are equivalent.
Since NRZI is a bipolar encoding, there is basically no DC current consumption. Moreover, the receiver automatically detects the presence of a signal because a zero voltage level never occurs during a transmission.

The weak point associated to the stand-alone NRZI encoding is that if there are too many 1-logic bits to be transmitted, a DC current component appears and the clock synchronization becomes more difficult. The solution adopted in HDLC is the bit stuffing procedure: after five 1-logic bits, a 0-logic bit is automatically inserted, then it will be removed at RX side (Figure 86).

Finally, frame delimiting refers to the flag insertion at the beginning/end of any frame. As previously exposed, such a bit pattern is not allowed within the user data and it is not subject to the bit-stuffing procedure.

A last remark refers to the polynomial scrambling, that is an algorithm for producing data encryption. Although it is not part of HDLC, it is usually implemented by many commercial modems. Such a technique allows to flip specific bits in order to make the message unintelligible, unless the receiver is equipped with a suitable descrambler.
The standard 9600 baud analogue MSK modem was designed by Miller in the 1980s and it uses the polynomial scrambling technique. Miller’s design, often referred to by his radio amateur callsign G3RUH, is based on the $1 + x^{12} + x^{17}$ polynomial.

As pointed out in Figure 88, scrambler and descrambler are closely related. As a matter of fact, they both apply modulo-2 additions according to the scrambling polynomial in order to either modify the sequence to be transmitted or restore the initial configuration.
5.5 **Keep It Simple, Stupid**

When radio amateurs started to experiment packet radio, the available computers had limited performance and were not able to implement the AX.25 protocol. The solution was to use dedicated external devices called TNC for providing both protocol and modem functions[3]. This approach was not flexible because the fixed firmware did not allow to perform any variation to the protocol. As far as computer performance improved, the need of a greater packet control rose up, then the KISS mode was developed in order to bypass the prefixed rules and use the TNC like a simple modem. In such a way the host can achieve the full control of the OSI stack, while in the past it was completely transparent.

The KISS-mode frame can be composed of an AX.25 packet with neither CRC nor HDLC encoding, then specific commands (CMD) are used to program the TNC.

| Frame | CMD | AX.25 datagram | Frame |

**Figure 89: KISS-mode frame**

If required, at TX side the TNC can compute the CRC and perform HDLC encoding, while at RX side the TNC will remove the HDLC encoding and validate the checksum before sending
the frame to the host. There is no standard for the list of available KISS-mode commands, but
the minimal requirements are listed in Figure 90.

- **Data frame** denotes that the rest of the frame is a data to be sent.
- **Transmitter keying delay** sets a TX delay for a time duration which is identified by the
  following byte (measured in 10 ms).
- **Persistence** causes the TNC to wait for an exponentially-distributed random interval before
  attempting to transmit (CSMA).
- **Slot interval** sets the slot interval duration as identified by the following byte (measured
  in 10 ms).
- **Full duplex** sets the transmission in half/full duplex mode;
- **Exit KISS mode** returns the channel control to a higher-level program.

Finally, the KISS-mode reserves several characters for its own purposes (Figure 91). For instance,
the FEND character delimits frames and if the corresponding pattern occurs in data, it is
replaced by the frame escape character FESC. Then, FESC is followed by the transposed frame end character TFEND in order to highlight the substitution. Similarly, if a FESC occurs in data, it is replaced by TFEND, then it is followed by the transposed frame escape character TFESC. The receiver must decode those characters and decides either to directly send information to the host, or store data and perform characters substitution before sending.
CHAPTER 6

HARDWARE DESIGN

In the chapter related to the parts selection, both the ICs and the main passive components were figured out. After that, the UML description was developed in order to share the electrical details and receive the approval by the project coordinators. The following step is to perform the complete hardware design in terms of schematics and printed circuit board, then that is the objective of this chapter. As previously mentioned, specific countermeasures are also discussed and taken in order to tackle the space environment related issues.

6.1 Schematics

6.1.1 Mentor Graphics

Once the part selection is completed, the following step consists in developing the physical board. In order to accomplish such a goal, the computer aided engineering software (CAE) Mentor Graphics is going to be used. Firstly, a central library must be created as a reference for all the components which have been previously selected. Each element is called part and consists of a physical cell (referring to the PCB) and a corresponding symbol (referring to the schematic). While the symbol is totally arbitrary (only the number of I/O pins must coincide with the real device), the cell has to be consistent with the actual package (e.g. SOIC, DIP, SIP, QFN). As a matter of fact, the padstack is created according to the required shape of both pads.
and holes, so in the end the electronic component will be correctly soldered over the specific support.

Each component is labeled according to its part number (i.e. vendor code) and part name (i.e. device typology), so it is uniquely identified. Then, the cell can be developed according to the mechanical structure of the device, by including *padstack*, *soldermask* and *silkscreen borderline*.

In any schematic, symbols are used to generate the electrical networks, while Mentor Graphics will automatically associate the corresponding cell according to the specific part.
Figure 93: Symbol - OPAMP5 SOIC package (Mentor Graphics environment)

Figure 94: SOIC package
6.1.2 Bill of Materials

In the following tables, a prefix identifies the specific vendor for each electronic component. *DK* stands for *Digi-Key*, *FR* stands for *Farnell* and *RS* stands for *RS-online-components*. In order to develop the electronic board, 131 components are required.
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<td>C_10N_0603_X7R_50V_10</td>
<td>C16-C21</td>
</tr>
<tr>
<td>56</td>
<td>1</td>
<td>DK-RHM.30STR-ND</td>
<td>R300m</td>
<td>R1</td>
</tr>
<tr>
<td>57</td>
<td>1</td>
<td>DK-296-21715-5-ND</td>
<td>TPS5450</td>
<td>U9</td>
</tr>
<tr>
<td>58</td>
<td>1</td>
<td>DK-INA138NACT-ND</td>
<td>OA_INA138</td>
<td>U6</td>
</tr>
<tr>
<td>59</td>
<td>1</td>
<td>FR-2066374</td>
<td>RF6886</td>
<td>U10</td>
</tr>
<tr>
<td>60</td>
<td>2</td>
<td>RS-301-322</td>
<td>p-MOSFET</td>
<td>Q1-Q2</td>
</tr>
<tr>
<td>61</td>
<td>1</td>
<td>RS-684-1273</td>
<td>NTC_100K_0603_1</td>
<td>R21</td>
</tr>
<tr>
<td>62</td>
<td>2</td>
<td>DK-NTA7002NTOSCT-ND</td>
<td>n-MOSFET</td>
<td>Q3-Q4</td>
</tr>
<tr>
<td>63</td>
<td>3</td>
<td>DK-LM317LD-ND</td>
<td>IC_REG 1.2V-37V</td>
<td>U3-U5</td>
</tr>
<tr>
<td>64</td>
<td>1</td>
<td>DK-296-19579-1-ND</td>
<td>CC1020</td>
<td>U8</td>
</tr>
<tr>
<td>65</td>
<td>1</td>
<td>DK-631-1070-2-ND</td>
<td>FOX924B</td>
<td>X3</td>
</tr>
<tr>
<td>66</td>
<td>1</td>
<td>DK-863-1174-1-ND</td>
<td>SKY13290-313LF</td>
<td>U1</td>
</tr>
<tr>
<td>67</td>
<td>1</td>
<td>RS-698-7001</td>
<td>MSP430F5438</td>
<td>U7</td>
</tr>
<tr>
<td>68</td>
<td>1</td>
<td>RS-1B127-Neohm</td>
<td>1B127-Neohm</td>
<td>U2</td>
</tr>
<tr>
<td>69</td>
<td>1</td>
<td>DK-J501-ND</td>
<td>SMA90</td>
<td>J1</td>
</tr>
<tr>
<td>70</td>
<td>1</td>
<td>RS-511-507</td>
<td>J6_20pin_SMT</td>
<td>J2</td>
</tr>
</tbody>
</table>
### TABLE XXXII: BILL OF MATERIALS 5/5

<table>
<thead>
<tr>
<th>ID</th>
<th>QTY</th>
<th>PART NUMBER</th>
<th>PART LABEL</th>
<th>REFERENCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>71</td>
<td>1</td>
<td>RS-JTAG14_PIN</td>
<td>JTAG_14pin</td>
<td>J3</td>
</tr>
<tr>
<td>72</td>
<td>1</td>
<td>DK-SE2418CT</td>
<td>Crystal_32kHz</td>
<td>X1</td>
</tr>
<tr>
<td>73</td>
<td>1</td>
<td>DK-631-1005-1-ND</td>
<td>Crystal_4MHz</td>
<td>X2</td>
</tr>
<tr>
<td>74</td>
<td>1</td>
<td>DK-478-3303-1-ND</td>
<td>C_220U_Tantal_16V_2917</td>
<td>C54</td>
</tr>
<tr>
<td>75</td>
<td>2</td>
<td>DK-445-3486-1-ND</td>
<td>C_47U_Y5V_25V_2220</td>
<td>C52-C53</td>
</tr>
<tr>
<td>76</td>
<td>1</td>
<td>DK-490-1313-1-ND</td>
<td>C_10N_Murata_16V_X7R</td>
<td>C24</td>
</tr>
<tr>
<td>77</td>
<td>2</td>
<td>RS-534-5730</td>
<td>C_10N_50V_X7R_0603</td>
<td>C50-C51</td>
</tr>
</tbody>
</table>

#### 6.1.3 Top schematics

The top-level circuit is depicted in Figure 96 and it is characterized by the OBC-RF module connector (J2), the main block containing the UHF telecommunication circuits and the antenna coaxial connector (J1).
Figure 96: Top Schematic (Mentor Graphics environment)
Figure 97: Schematic1 - Overall view (Mentor Graphics environment)
Figure 98: Schematic 1 - Region A (Mentor Graphics environment)
Figure 99. Schematic 1 - Region B (Mentor Graphics environment)
Figure 100: Schematic - Region C (Mentor Graphics environment)
Figure 101: Schematic - Region D (Mentor Graphics environment)
Figure 102: Schematic1 - Region E (Mentor Graphics environment)
6.1.4 Transceiver

Figure 103: Transceiver - Overall view (Mentor Graphics environment)
Figure 104: Transceiver - Region A (Mentor Graphics environment)
Figure 105: Transceiver - Region B (Mentor Graphics environment)
Figure 106: Transceiver - Region C (Mentor Graphics environment)
Figure 107: Transceiver - Region D (Mentor Graphics environment)
6.1.5 Tile processor

Figure 108: Tile processor - Overall view (Mentor Graphics environment)
Figure 109: Tile processor - Region A (Mentor Graphics environment)
Figure 110: Tile processor - Region B (Mentor Graphics environment)
Figure 111: Tile processor - Region C (Mentor Graphics environment)
Figure 112: Tile processor - Region D (Mentor Graphics environment)
6.2 PCB

6.2.1 Surface Mount Technology

SMT is a method for building up electronic circuits where components are directly mounted onto the PCB surfaces. In the industrial processes, such a method has largely replaced the through-hole technology (THT), which was based on plugging components through the PCB holes. As a matter of fact, an SMD component is usually smaller than the THT counterpart because it has no lead wires. In contrast, SMDs have short pins or various styles leads, such as flat contacts or a matrix of solder ball terminations (BGA).

The locations where components must be placed are normally silver/gold/copper pads without holes (solder pads). Solder paste, a mixture of tiny solder particles, is firstly applied over the solder pads, then boards proceed to the pick-and-place machines. At the same time, the electronic components are usually delivered to the production line through either paper/plastic tapes or plastic tubes. Then, numerical controlled pick-and-place machines pick the parts from the tapes/tubes and place them on the PCB. Finally, the boards are conveyed into soldering ovens. At that point, the surface tension of the molten paste automatically aligns the components on the respective pads. If the circuit board is double sided, the process may be repeated once again.

The main advantages of SMT over the older through-hole technique are:

- the presence of smaller components (down to $0.2 \times 0.1 \text{ mm}^2$) allows a much higher integration;
- small errors in the component placement are automatically corrected in the ovens;
Figure 113: Example of SMT applied to PCB

- components can be placed over both sides of the PCB;
- there are lower parasitic inductances (i.e. better performance for RF circuits);
- there are better mechanical performance against vibration (very useful in space applications);
- there are lower EM emissions as a consequence of both smaller radiation loop areas (because of the smaller packages) and smaller lead inductances;
- the assembly process is much faster (up to 136,000 components per hour).

The electronics industry has also standardized packages. For instance, the 2-terminals components (e.g. capacitors, resistors, inductors) may have the following dimensions:

\[ \text{Code 0402} \implies 40 \text{ mil} \times 20 \text{ mil} \approx 1 \text{ mm} \times 0.5 \text{ mm} \]
Code 0603 $\Rightarrow$ 60 mil $\times$ 30 mil $\approx$ 1.5 mm $\times$ 0.75 mm

6.2.2 Stack-up

PCBs are usually made of multiple layers where metal traces (e.g. copper) are separated by dielectrics (e.g. FR-4). In this thesis, the reference which is going to be considered for the implementation of the electronic board is depicted in Figure 114.

As a matter of fact, that is the standard stack-up provided by *Eurocircuits corporation* and following the manufacturer’s standard is the starting point for a low-cost product. In this thesis, a stack-up composed of 6 layers is selected because it allows to separate critical paths and manage a large number of digital connections.
The first layer is mainly used to place electronic components and radio frequency traces. Since both length and width associated to the traces dramatically affect characteristic impedances and RF power fading, this is the most constrained layer. Moreover, any attempt of surface optimization fully depends on the components disposition over such a layer. In order to avoid EM coupling, RF traces must be surrounded by ground planes and that is the reason why all the regions which are not occupied by any component are filled with metal.

The second and the fifth layers are analog GND planes, while the third plane is the 3.3 V one. It is important to select sufficiently stable voltages for the plane assignment in order to avoid that any metal plane acts as a patch antenna. Regarding this, both GND and 3.3 V power supply are stable voltages, so they are suitable targets. Additionally, they are referred by many nets in the project, so those selections allow to reduce the number of metal traces.

All the other copper made layers are assigned for digital signals only. As a result, they are not very constrained and the reason why more layers have been selected is just to reduce the number of vias.

A last remark refers to the substrate layers (FR-4) because there is a difference between core and prepreg in terms of construction. In the PCB stack-up, the core layers are directly provided by the manufacturer with two adjacent metal layers (e.g. copper-2, core, copper-3). In contrast, all the other metal layers are grown over prepreg substrates, then they are glued over already existing core structures.
6.2.3 Boards for space applications

When developing electronic boards devoted to space applications, some specific precautions must be considered in order to prevent failures and damages.

Firstly, the Joule effect produces thermal energy which must be dissipated outside by all the electronic devices. Regarding this, the following calculations allow to quantify the temperature difference produced by a lumped dissipative element. The infinitesimal temperature difference \((dT)\) is related to the dissipated power \((P)\), to the specific thermal resistivity of the support \((\rho)\) and to the circular surface which contains the lumped element[14].

\[
dT = P\rho \frac{dr}{S(r)}
\]

Hence, the temperature difference between a generic point on the PCB \((R_b)\) and the boundary associated to dissipative component \((R_a)\) is:

\[
\Delta T = \int_{R_a}^{R_b} P\rho \frac{dr}{S(r)} = P\rho \int_{R_a}^{R_b} \frac{1}{2\pi rh} dr = \frac{P\rho}{2\pi h} \int_{R_a}^{R_b} \frac{1}{r} dr = \frac{P\rho}{2\pi h} ln \left( \frac{R_b}{R_a} \right).
\]

The partial vacuum and the consequent lack of heat dissipation by convection require different approaches to dissipate thermal energy. As a matter of fact, the objective is to dissipate
TABLE XXXIII: THERMAL ANALYSIS OVER STANDARD PCB MADE OF FR-4

<table>
<thead>
<tr>
<th>Component</th>
<th>$P_{\text{max}}$ [W]</th>
<th>$\Delta T$ [$^\circ$C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA - RF6886</td>
<td>5.2</td>
<td>5.76</td>
</tr>
<tr>
<td>LNA - CXE2089Z</td>
<td>1.2</td>
<td>1.33</td>
</tr>
</tbody>
</table>

$R_B - R_a = 5 \text{ cm}$

$h = 1.5 \text{ mm}$

energy by irradiation through the external tiles of the satellite. That is crucial to keep $\Delta T$ within the safe operating region of the electronic board. The only way to achieve such a goal is to take advantage from heat conduction by means of physical connections among components and the external surfaces\footnote{Energy and Thermal Management in Space: Design and Application to Satellite Systems}. For example, thermal bridges are metal strips which allow to keep in contact electronic components with the external structure, but they are feasible only for few devices. As a matter of fact, it is preferable not to add too much additional weight and because components must be sufficiently large to support the specific mechanical connections. Secondly, heat pumps use mechanical work to accomplish the desired transfer of thermal energy from a source to the sink. This technology is commonly adopted in terrestrial applications (e.g. air conditioners), but it is very expensive in space applications since vapor-compression-refrigeration cycles require pressurized pipes in order to prevent explosions. Finally, the solution which provides more benefits consists in exploiting the conducting capability of both ground and voltage supply planes. As a matter of fact, they are already present inside the PCB and do not require additional efforts. Once PCBs are mounted onto the metallic structure of the satellite (A1) by
means of specific turrets, the intermediate volume must just be filled with conducting carbon rubber (Figure 116).

In this way, it is firstly possible to cover both layers with SMDs without losing accessibility since filler is easily removable. Secondly, the rubber filler allows heat dissipation toward the external structure, remaining tolerant to slightly different expansions between PCB and aluminum panels. In facts, PCB is made of FR-4 (fiberglass cloth with an epoxy resin) and it has a thermal expansion coefficient different from aluminum, so if the connection was direct (without rubber filler), the board would detach through the action of extension/compression movements.

Furthermore, placing the most dissipative components as close as possible to the metallic turrets leads to an even faster heat dissipation.

Some other precautions must be considered to tackle vibration issues during the launch. From a structural point of view, both acoustic and conducting vibrations can be studied as accelerations applied over any electronic device (up to 10G). Figure 117 shows a generic surface mounted component placed onto a portion of PCB optimized for thermal dissipation.
Since vibrations are spurious and affect the entire range of frequencies (up to 20 KHz), the structure definitely acts as a mechanical resonator and the coefficient $Q$ amplifies the normal acceleration onto the device[14]. Acceleration leads to either traction or compression strengths according to its own verse (respectively positive and negative). Although compression is completely balanced by the mechanical reaction of a PCB with a suitable thickness, traction directly affects the device-pad-PCB connection. As a result, the maximum pressure ($p_{\text{max}}$) can be estimated and a suitable glue can be added to prevent component detaching.

$$p_{\text{max}} = \frac{F}{S_{\text{contact}}} = \frac{m_{\text{device}}aQ}{S_{\text{contact}}}$$

As pointed out by the foregoing formula, if $p_{\text{max}}$ is too high for all commercial glues (beyond MPa), it is possible to reduce its value by enlarging $S_{\text{contact}}$. Moreover, huge accelerations intrinsically lead to huge growths in the weight of each component, so placing high mass devices close to the turrets is a good choice to preserve the PCB integrity. Interconnections among different boards are also critical due to vibrations, then the anchoring procedure for mobile wires is a necessary condition to prevent dangerous oscillations. Additionally, metal cables tend
to weaken and break under action of the tens bendings per second caused by vibrations. As shown in Figure 118, in order to minimize such a hazard, either connectors or strain reliefs can be used.

Beyond thermal and vibration issues, there are also problems related to dielectrics perforation and oxidation/deoxidation processes. Since the relative permittivity in space environment is $\varepsilon_r = 1$ (vacuum), while under standard terrestrial conditions it is slightly higher, sparks can occur in an easier way with the consequent PCB burning. The solution is to cover metal traces with resins and use PCB made of kapton because such a polyimide is much more resistant than FR-4 to both thermal variations and burns. On the other hand, oxidation affects the external metal components because monatomic oxygen orbiting at high speed (about $10^7$ km/s in LEO) is very reactive. In order to prevent oxidation of electronic components, gold-plated connectors should be used and, once again, metal traces should be covered with protective resins. Additionally, although oxidation produces $Al_2O_3$ (alumina) on the external structural surfaces, under vacuum conditions deoxidation takes place. As a consequence, pure aluminum powder
originates from the alumina and, under action of gravitational force, it also tends to settle over external circuitry causing short circuits. However, chromium plating conversion of the aluminum planes (alodine) definitely protects the structure from those chemical reactions[14].

6.2.4 RF traces

In order to avoid impedance mismatch among radio frequency units, it is necessary to design suitable metal traces. Table XXXIV reports the main parameters associated to the materials which are going to be used in the PCB.

<table>
<thead>
<tr>
<th>Name</th>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>$\sigma$</td>
<td>$5.88 \cdot 10^7 , \text{S} / \text{m}$</td>
</tr>
<tr>
<td>Mohs hardness</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td></td>
<td>$3.1 \cdot 10^6 , \text{A} / \text{m}^2$</td>
</tr>
<tr>
<td>Thickness</td>
<td></td>
<td>20 $\mu$m</td>
</tr>
<tr>
<td>Density</td>
<td></td>
<td>$1850 , \text{Kg} / \text{m}^3$</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td></td>
<td>4.7</td>
</tr>
<tr>
<td>FR-4</td>
<td>$\rho$</td>
<td>$10^9 , \text{M}\Omega \cdot \text{m}$</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td></td>
<td>$&gt; 50 , \text{KV}$</td>
</tr>
<tr>
<td>Loss tangent</td>
<td></td>
<td>0.002</td>
</tr>
<tr>
<td>Thickness</td>
<td></td>
<td>0.2 mm</td>
</tr>
</tbody>
</table>

Since both the input and the output impedances associated to the RF electronic modules are equal to 50 $\Omega$, the characteristic impedance of the microstrips must be 50 $\Omega$. In fact, that
allows to ensure negligible reflection coefficients (|Γ|). *AWR-TXLINE* tool allows to design a physical microstrip starting from the set of parameters previously collected.

\[
\Gamma = \frac{Z_{\text{load}} - Z_0}{Z_{\text{load}} + Z_0}
\]

As a result, the microstrip must be approximately 352 µm wide, independently from the physical length.

Similarly, impedance matching must be ensured also for the connection between the radio frequency switch and the antenna connector, where a 220 pF capacitor has been placed for decoupling purposes. By using *AWR DESIGN ENVIRONMENT*, it is possible to compute the variation in the return loss due to the capacitance uncertainty.

According to the PCB specifications (collected in Figure 119) and assuming a 5% accuracy for the capacitor, the return loss is lower than −40 dB, then such a phenomenon can be neglected.
6.2.5 Top-level PCB

According to the AraMiS mechanical constraint (165x165 mm$^2$), the physical size corresponding to the board must not exceed those dimensions. Since just the UHF channel has been developed, only half of the available surface can be actually occupied. According to such a space constraint, the final PCB is going to be a 6-layers 113x65 mm$^2$ rectangle (gerber profiles are reported in Appendix H).
Figure 121: Complete PCB (Mentor Graphics environment)
Figure 122: PCB without traces and planes (Mentor Graphics environment)
### TABLE XXXV: LEGEND FOR THE PCB DESCRIPTION

<table>
<thead>
<tr>
<th>Description</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>White</td>
</tr>
<tr>
<td>Layer 4</td>
<td>Bright green</td>
</tr>
<tr>
<td>Layer 6</td>
<td>Brown</td>
</tr>
<tr>
<td>Silkscreen</td>
<td>Pink</td>
</tr>
<tr>
<td>Component outline</td>
<td>Dark green</td>
</tr>
<tr>
<td>Solder-mask</td>
<td>Light green</td>
</tr>
<tr>
<td>Reference designator</td>
<td>Orange</td>
</tr>
</tbody>
</table>
CHAPTER 7

SOFTWARE DESIGN

In this chapter the entire software architecture is going to be designed in terms of protocol management and housekeeping functions. All the methods devoted to program the transceiver according to the project specifications and the Packet Radio description are firstly provided. Then, the housekeeping array containing the sensors data is periodically monitored and the SPI-interface with the OBC/transceiver is established. In this context, the Visual Paradigm environment is not only used for the UML description, but also for the automatic code generation. In order to contrast the radiation effects, a specific software hardening based on the variable triplication is also designed.

7.1 Reliability

Since the control software is destined to a space application, ensuring a sufficiently long-term reliability is a crucial design feature. As a matter of fact, due to both the impossibility of reaching the spacecraft for repairs and the high mission cost, it is not tolerated any failure within the predefined lifetime. That is valid for all the aspects associated to the AraMiS system (e.g. mechanical structure and electronic boards), so also the software design must be fault tolerant.

Once a fault occurs, any system can react in three different ways according to its quality of design and the availability of resources. Firstly, a fail-operational does not affect the overall
system because all tasks continue to be pursued and basically the fault is transparent to the end user. That happens in case of redundancy because once a module crashes, an equivalent one takes its place and completely substitutes the first. Secondly, a *fail-safe* occurs when despite the failure the system still remains in the working status, but lower performance is allowed. Finally, a *fail-stop* arises when the failure leads the system to a complete crash.

Although there is no chance to keep any system in a permanent fault-operational condition, there are some design directives to increase the software robustness. Firstly, SEUs cause bit flips in the central memory, so the smaller the data structure, the lower the probability that the bit flip encounters an allocated memory cell. As a result, the *data-type optimization* is crucial in order to save memory space and reduce error probability. As a result, it is strongly recommended to avoid the use of both “integer” (32 bits) and “double” (64 bits) whenever either “char” (8 bits) or “short” (16 bits) are sufficient.

\[
p_e = p_{SEU} \cdot \text{sizeof}(T) \cdot T_V
\]

The previous formula allows to compute the worst-case error probability \(p_e\) as a function of three parameters: the SEU probability \(p_{SEU}\), the length of the variable \(\text{sizeof}(T)\) and the cycle of the variable \(T_V\). The latter is the maximum timeframe between two adjacent writing operations of the same variable \(T\).

Moreover, in order to tackle SEUs it is recommended to use *redundancy* and store the same value into three different locations whenever a write-operation occurs. In fact, since it is very unlikely that two out of three data are wrong, an algorithm based on the majority voting should always detect the correct value. Even though redundancy requires periodic variables refresh to
reduce $T_V$ and it leads to slower reading/writing operations, such a method is however faster than any CRC computation. Data duplication can be achieved by means of either multiple supports (e.g. RAID) or different variables allocated in the same support. In the latter case, the compiler must not optimize variables in the source code. As a matter of fact, different variables carrying the same value would be mapped over the same memory cell, canceling the effect of redundancy.

In the AraMiS architecture specific software classes are implemented to easily handle variable redundancy. Figure 123 shows an example of class (TripleBool) which allows to automatically use three different Boolean variables ($d_1$, $d_2$ and $d_3$) carrying the same information. All standard operations have been redefined so that any operation, any majority vote and any refresh-synchronization over the three variables take place just by calling one specific method.

Figure 123: Triple Boolean software-class (Visual Paradigm)
% Example of operations with triple variables%

result.d1 &= val.d1;  // AND operation over variable d1
result.d2 &= val.d2;  // AND operation over variable d2
result.d3 &= val.d3;  // AND operation over variable d3
return result;

// Triple variable vote.
if (this->d1==this->d2)
    return this->d1;
else if (this->d1==this->d3)
    return this->d1;
else if (this->d2==this->d3)
    return this->d2;
else
    return trap();  // i.e. return 0 (no data recovery)

// Triple variable synchronization during refresh.
if (this->d1 == this->d2) {
    if (this->d1 == this->d3) {
        return this->d1;
    }
    else {
        this->d3 = this->d1;
        return this->d1;
    }
}
else {
    if (this->d1 == this->d3) {
        this->d2 = this->d1;
        return this->d1;
    }
    else if (this->d2 == this->d3) {
        this->d1 = this->d3;
        return this->d2;
    }
    else
        return trap();
}
Secondly, in order to minimize errors during calculations, a useful rule is to employ integer arithmetic instead of the floating point one. That is because integer operations are less time consuming, then the probability that an error affects the final result is lower.

Furthermore, SEUs lead to differently critical faults according to the memory cell they may affect. For example, assuming the following statement, a SEU can modify either the pointer $(vet)$ or one of the two variables $(a, b)$.

\[ vet[a] = b; \]

In case of error on $b$, consequences are not very dangerous because just a redundancy mechanism over the entire vector can easily correct the mistake. In contrast, in case the error affects either $vet$ or $a$, the value associated to $b$ could modify a system memory location (e.g. either interrupt enable/disable or reset) causing a fatal system crash. In order to avoid those eventualities, it is recommendable to declare as many constant numbers as possible (e.g. \#define a 4) because they are supposed to be stored in the ROM, then safe from any SEU.

A last remark refers to the loops construction and the bad boundaries definition. Regarding this, it may happen that a SEU leads the overall system to an unknown state with the consequent system crash.

\[ \text{while(wait())} \{ ... \} \]

The previous statement is a while-loop which stalls the system until the function $wait()$ returns 0. However it does not take into account that, if the function will never return such a value, the system is going to remain in the waiting mode forever. A suitable countermeasure is
to design a watchdog counter in order to have a second condition for breaking the loop. Similar unexpected situations also come from bad boundary definitions, as shown by the following statement.

\[
if(a < length(str)) str[a] = 'b';
\]

As a matter of fact, the program can be designed in such a way that \( a \) is always positive, so checking that its value is lower than the length of the vector seems to be sufficient. However, \( a \) could become negative as a consequence of a SEU, then the statement \( str[a] = 'b' \) would lead the system to a crash condition. In order to avoid that issue, it is recommendable to always define both the upper and the lower boundary.

### 7.2 Ports

Before starting to program the microcontroller, it is necessary to identify the ports of processor which are actually connected in the board.

According to Table XXXVI, it is possible to refer to any interface by software routines.

### 7.3 CRC algorithms

The native implementation for computing and checking a CRC is the *bit-based* approach and that is the first algorithm which is going to be implemented. The MSP430 microcontrollers can do the bit-by-bit division very well, however they are much more efficient at handling data in bytes or words. Regarding this, a *table-based* solution is pointed out as well.

The bit method is just a binary polynomial division where the remainder is conserved, while the quotient is discarded. After the computation, the remainder is then appended to the message
in order to form the code word. Such a bitwise procedure is based on the Linear Feedback Shift
Register (LFSR) previously described. The algorithm consists of the following steps:

- initialize the CRC register \((FFFF)\);
- shift the CRC left by one bit while shifting in the next message-bit;
- if the bit just shifted out is set, XOR the CRC with the generator polynomial;
- continue with step 2 until there are no message-bits left;
- XOR the CRC register with the final XOR value.

TABLE XXXVI: PORTS MAPPING BETWEEN THE MICROCONTROLLER AND THE OTHER UNITS

<table>
<thead>
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% Library for both CRC implementations %

//CRC-CCITT description

#define POLYNOMIAL 0x1021
#define INITIAL_REMAINDER 0xFFFF
#define FINAL_XOR_VALUE  0x0000
#define REFLECT_DATA FALSE
#define REFLECT_REMAINDER FALSE

/*******************

#define FALSE 0
#define TRUE !FALSE

typedef unsigned short crc;

//Derive parameters from the standard-specific parameters in crc.h.
#define WIDTH (8 * sizeof(crc))
#define TOPBIT (1 << (WIDTH - 1))

#if (REFLECT_DATA == TRUE)
#define REFLECT_DATA(X) (((unsigned char) reflect((X), 8)))

#define REFLECT_REMAINDER(X) (((crc) reflect((X), WIDTH)))

/* Description: Reorder the bits of a binary sequence, by reflecting them about the middle position. */

/* Returns: The reflection of the original data. */

static unsigned long
reflect(unsigned long data, unsigned char nBits)
{
    unsigned long reflection = 0x00000000;
    unsigned char bit;

    /*
     * Reflect the data about the center bit.
     */
    for (bit = 0; bit < nBits; ++bit)
    {
        /*
         * If the LSB bit is set, set the reflection of it.
         */
        if (data & 0x01)
        {
            reflection |= (1 << ((nBits - 1) - bit));
        }
        data = (data >> 1);
    }
    return (reflection);
}
% bitWise CRC implementation %

/**************************************************************************/

/* Description: Compute the CRC of a given message (message[]) and its length (nBytes).

* Returns: The CRC of the message.
****************************************************************************/

crc crcBitWise(unsigned char const message[], int nBytes)
{
    crc remainder = INITIAL_REMAINDER;
    int byte;
    unsigned char bit;

    /*
    * Perform modulo-2 division, a byte at a time.
    */
    for (byte = 0; byte < nBytes; ++byte)
    {
        /*
        * Bring the next byte into the remainder.
        */
        ...
/
remainder ^= (REFLECT_DATA(message|byte)) << (WIDTH - 8));

/*
 * Perform modulo-2 division, a bit at a time.
 */
for (bit = 8; bit > 0; --bit)
{
    /*
     * Try to divide the current data bit.
     */
    if (remainder & TOPBIT)
    {
        remainder = (remainder << 1) ^ POLYNOMIAL;
    }
    else
    {
        remainder = (remainder << 1);
    }
}
In contrast, the advantage of the table method is that CRC values can be pre-calculated and stored in a data structure (e.g. flash memory). The table algorithm presented uses table sizes of 256 words to balance between MIPS (power consumption) and memory. As a trade-off, the larger the table, the lower the computational cost and the larger the memory allocation. The algorithm consists of the following steps:

- initialize the CRC register ($FFFF$);
- XOR the CRC most significant byte with the incoming message-byte;
- use this byte to index into the 256 entry table;
- shift the CRC register to the left by one byte;
- XOR the CRC register with the value indexed into the table;
- Continue with step 2 until no more message bytes are left;
- XOR the CRC register with the final XOR value.
In the AX.25 framework, the algorithm is called *CRC-CCITT* and the generator polynomial is $x^{16} + x^{12} + x^5 + 1$ (the hexadecimal notation is 0x1021).

% % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % %
% byteWise CRC implementation %
% % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % %

//////////////////////////////////////////////////////////////////////////

* Description: Populate the partial CRC lookup table.
* Returns: None defined.

/////////////////////////////////////////////////////////////////////////

crc crcTable[256];

void crcInit(void)
{

crc remainder;

int dividend;

unsigned char bit;

/*

* Compute the remainder of each possible dividend.

*/

for (dividend = 0; dividend < 256; ++dividend)
{

    /*
     * Start with the dividend followed by zeros.
     */

    remainder = dividend << (WIDTH - 8);

    /*
     * Perform modulo-2 division, a bit at a time.
     */

    for (bit = 8; bit > 0; --bit)
    {
        /*
         * Try to divide the current data bit.
         */

        if (remainder & TOPBIT)
        {
            remainder = (remainder << 1) ^ POLYNOMIAL;
        }

        else
        {
            remainder = (remainder << 1);
        }
    }
/ *
   * Store the result into the table.
   * /
   crcTable[dividend] = remainder;

} }

/****************************
* Description: Compute the CRC of a given message.
* Notes:                     crcInit() must be called first.
* Returns:                   The CRC of the message.
****************************/
crc crcByteWise(unsigned char const message[], int nBytes)
{
    crc remainder = INITIAL_REMAINDER;

    unsigned char data;

    int byte;
/∗ 
 * Divide the message by the polynomial, a byte at a time.
 */

for (byte = 0; byte < nBytes; ++byte)
{
    data = REFLECT_DATA(message[byte]) ^ (remainder >> (WIDTH - 8));
    remainder = crcTable[data] ^ (remainder << 8);
}

/*
 * The final remainder is the CRC.
 */

return (REFLECT_REMAINDER(remainder) ^ FINAL_XOR_VALUE);
Figure 124: Software architecture - Overall view (Visual Paradigm)
Figure 125: Software architecture - Region A (Visual Paradigm)
Figure 126: Software architecture - Region B (Visual Paradigm)
Figure 128: Software architecture - Region D (Visual Paradigm)
Figure 129: Software architecture - Region E (Visual Paradigm)
Figure 130: Software architecture - Region F (Visual Paradigm)
Figure 131: Software architecture - Region G (Visual Paradigm)
Figure 132: Software architecture - Region H (Visual Paradigm)
According to the UML architecture, the Bk1B31A1S-OBRF-437MHz software class includes the main available functions. They are based on the methods which are listed in Appendix J/K/L/M. In the following list, each method is going to be documented.

\textit{boot() : void.} Whenever the module is reset (or enabled after a period in which it was disabled, i.e. switched off), it is the first function to be called. It stops the watch-dog timer, it initializes the tile processor and increments the boot-counter (e.g. for detecting the number of occurred SEUs).

\begin{verbatim}
% boot() : void

    WDTOCTL = WDTPW + WDT HOLD;  // Stop watchdog timer
to prevent time out reset

    processor.init();  // processor initialization

    // Flash management for storing the number of reboots due to latch-up
    flash.initiateWrite();
    flash.write(flash.INFO_A_first, (byte)
\end{verbatim}
(flash.read(flash.INFO_A_first)+1)); // increase the boot-counter by 1
flash.terminateWrite();

uC-LPM(mode : $MSP-430.t-LPModes : void). Sets the microcontroller in Low Power Mode/Active Mode according to the MSP430 modes enumeration.

resetFlash() : void. Resets to zero the FLASH memory location where the number of reboots is stored.

flash.initiateWrite();
flash.write(flash.INFO_A_first,(byte)(0));
flash.terminateWrite();
housekeeping(index : ushort) : void. Allows housekeeping functions and it must be called after initADCforHousekeeping(): void.

```cpp
switch (index) {
    case GET_PDB_VOLTAGE:
        module_interface.IOmodule_MSP_D<CPU_DESCRIPTOR2>.A0.
        acquire(HK::housekeeping[GET_PDB_VOLTAGE]);
        break;

    case GET_3V0_VOLTAGE:
        module_interface.IOmodule_MSP_H<CPU_DESCRIPTOR2>.A0.
        acquire(HK::housekeeping[GET_3V0_VOLTAGE]);
        break;

    case GET_2V8_VOLTAGE:
        module_interface.IOmodule_MSP_B<CPU_DESCRIPTOR2>.A0.
        acquire(HK::housekeeping[GET_2V8_VOLTAGE]);
        break;
}
```
case GET_3V3_VOLTAGE:
    acquire(HK::housekeeping[GET_3V3_VOLTAGE]);
break;

case GET_3V_POWER_VOLTAGE:
    acquire(HK::housekeeping[3V_POWER_VOLTAGE]);
break;

case GET_PA_TEMPERATURE:
    module_interface.IOmodule_MSP_C<CPU_DESCRIPTOR2>.A0.
    acquire(HK::housekeeping[GET_PA_TEMPERATURE]);
break;

case GET_CURRENT:
    acquire(HK::housekeeping[GET_PA_CURRENT]);
break;
case GET_LATCHUP_NUMBER:

    HK::housekeeping [GET_LATCHUP_NUMBER] = flash.read

    (flash.INFO_A_first);

break;

}

setSPI-cc1020() : void. Sets the SPI interface with the CC1020, where the microcontroller
is the master, while the transceiver is the slave. Before using it, it is necessary to initialize the
processor.

% setSPI_cc1020() : void

uartA0.init(MSP430::SPI_MASTER_MODE, Matheoud::CPU_DESCRIPTOR2.
UARTA0_BAUDRATE); //set processor in SPI master mode to handle
the transceiver

uartA0.enable(MSP430::SPI_MASTER_MODE); //enable the interface

setSPI-OBC() : void. Sets the SPI interface with the OBC, where the microcontroller is the
slave, while OBC is the master. Before using it, it is necessary to initialize the processor.
% setSPI_OBC() : void

uartB2.init(MSP430::SPI_SLAVE_MODE, Matheoud::CPU_DESCRIPTOR2, UARTB2_BAUDRATE); // set processor in SPI master mode to handle the transceiver
uartB2.enable(MSP430::SPI_SLAVE_MODE); // enable the interface

initADCforHousekeeping() : void. Initializes the ADCs A2, A3, A4, A5, A6, A12, A15. The reference voltage is 2.5 V and the sampling time is samplingTime : short. Before using it, it is necessary to initialize the processor.

% initADCforHousekeeping() : void

adc.enable();
adc.init(samplingTime, MSP430::VREF_2_5, 36988);

stopADC() : void. Turns off ADCs, disables their reference and any conversion. Before using it, it is necessary to initialize the processor.
\% stopADC(): \textbf{void}

\texttt{adc\_disable();}

\begin{verbatim}
\% % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % %
enablePA(): \textbf{void}. Enables power amplification. Before using this method, it is necessary to call \texttt{initGPIO(): void}.
\end{verbatim}

\begin{verbatim}
\% enablePA(): void
\end{verbatim}

\texttt{io\_driver <10,2,false>.\texttt{set();}}

\begin{verbatim}
\% % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % % %
initGPIO(): \textbf{void}. Initializes all the required GPIOs:
\end{verbatim}

\begin{itemize}
  \item 6 backdoor pins (OUT), to J6-interface;
  \item backdoor reset (OUT), to J6-interface;
  \item HZ1 for RF isolation (OUT), to J6-interface;
  \item DCLK interrupt (IN), from CC1020;
  \item DIO (IN/OUT) is not configured, from/to CC1020;
  \item LOCK (IN), from CC1020;
  \item PA-EN (IN), from CC1020;
\end{itemize}
- LNA-EN (IN), from CC1020;

- PowerStages (OUT), to the load switch for enabling/disabling power stages.

Before using it, it is necessary to initialize the processor:

```c
% initGPIO() : void

io_driver<1,128,false>.input(); // set DCLK as input
io_driver<1,128,false>.interruptEnable(); // activate

io_driver<4,1,false>.output(); // Set backdoor pin0 as output
io_driver<4,2,false>.output(); // Set backdoor pin1 as output
io_driver<4,4,false>.output(); // Set backdoor pin2 as output
io_driver<4,8,false>.output(); // Set backdoor pin3 as output
io_driver<4,16,false>.output(); // Set backdoor pin4 as output
io_driver<4,32,false>.output(); // Set backdoor pin5 as output
io_driver<4,64,false>.output(); // Set backdoor pin reset as output
io_driver<4,128,false>.output(); // Set HZ1 as output
```
io_driver<10,1,false>.input(); //Set LOCK as output

io_driver<10,2,false>.input(); //Set PA_EN as output

io_driver<10,4,false>.input(); //Set LNA_EN as output

io_driver<10,8,false>.output(); //Set the pin for power amplification enable as output

setDIO-in() : void. Sets the DIO signal coming from CC1020 as an input for the microcontroller. Before using it, it is necessary to initialize the processor.

setDIO-out() : void. Sets the DIO signal coming from CC1020 as an output for the microcontroller. Before using it, it is necessary to initialize the processor.
**disablePA() : void.** Disables power amplification. Before using this method, it is necessary to call `initGPIO() : void`.

```plaintext
io_driver<10,2,false>.reset();
```

**isLock() : bool.** Returns true if the PLL is locked. It return false whether the PLL is not locked. Before using it, it is necessary to initialize the processor and the transceiver.

```plaintext
return(io_driver<10,1,false>.read());
```

**isTX() : bool.** Returns true if the transceiver is set in TX mode. Before using it, it is necessary to initialize the processor and the transceiver.

```plaintext
return(io_driver<10,2,false>.read());
```
isRX() : bool. Returns true if the transceiver is configured in RX mode. Before using it, it is necessary to initialize the processor and the transceiver.

```c
return (io_driver < 10,4, false >.read ());
```

configCC1020() : void. Initializes the transceiver, sets the modulation technique (GFSK), sets the data format (NRZI) and the baudrate (9600 bps). Before using it, it is necessary to initialize the processor.

```c
cc1020.init ();
cc1020.Baud_rate=CPU_DESCRIPTOR2.UARTA0_BAUDRATE; // 9600 bps
cc1020.SetReg (0x01, 0xF);  
cc1020.SetReg (0x02, 0xFF);  
cc1020.SetReg (0x03, 0x8F);  
cc1020.SetReg (0x04, 0x3A);  
```
cc1020.SetReg(0x05,0x7A);
cc1020.SetReg(0x06,0xF1);
cc1020.SetReg(0x07,0x39);
cc1020.SetReg(0x08,0x3A);
cc1020.SetReg(0x09,0x85);
cc1020.SetReg(0x0A,0x9D);
cc1020.SetReg(0x0B,0x39);
cc1020.SetReg(0x0C,0x44);
cc1020.SetReg(0x0D,0x50);
cc1020.SetReg(0x0E,0xAB);
cc1020.SetReg(0x0F,0xC6);
cc1020.SetReg(0x10,0x2B);
cc1020.SetReg(0x11,0x61);
cc1020.SetReg(0x12,0x55);
cc1020.SetReg(0x13,0x2E);
cc1020.SetReg(0x14,0x29);
cc1020.SetReg(0x15,0x23);
cc1020.SetReg(0x16,0x78);
cc1020.SetReg(0x17,0x47);
cc1020.SetReg(0x18,0x14);
cc1020.SetReg(0x19,0x22);
cc1020.SetReg(0xA,0xAE);
cc1020.SetReg(0xB,0x34);
cc1020.SetReg(0xC,0xF0);
cc1020.SetReg(0xD,0x00);
cc1020.SetReg(0xE,0x00);
cc1020.SetReg(0xF,0x00);
cc1020.SetReg(0x20,0x00);
cc1020.SetReg(0x21,0x4D);
cc1020.SetReg(0x22,0x10);
cc1020.SetReg(0x23,0x06);
cc1020.SetReg(0x24,0x00);
cc1020.SetReg(0x25,0x40);
cc1020.SetReg(0x26,0x00);
cc1020.SetReg(0x27,0x00);

LPM_cc1020() : void. Sets the transceiver in low power consumption. In order to wake up the unit, configCC1020(): void must be called.

% LPM_cc1020() : void
buildPacket(message : char*, nByte : int, packet : char*, frameType : bool, addressType : bool, controlType : bool) : int. Builds the packet according to the protocol format. It returns the length of the packet. Before using it, it is necessary to initialize the processor.

```c
 int packetSize = nByte + 4; // packet length
 char addressLength; // length of the address field
 char controlLength; // length of the control field
 char* tmp; // supporting pointer
 char flag = 126; // flag

 // allocate memory for the final packet
 char* packet = (char*) malloc(packetSize * sizeof(char));
 if (ptr == NULL) {
   return 0; // error in malloc
```
tmp=packet;

(unsigned char) (*(tmp))=flag; //open the packet with the flag

//append the message to the packet and increment the supporting pointer
for (int cont=1; cont<=nByte; cont++)
    *(++tmp)=message[cont-1];

//compute and append CRC
(unsigned short) *(++tmp)=crcByteWise(message, nByte);

(unsigned short) *(tmp++); //increment the supporting pointer
(unsigned char) *(tmp)=flag; //close the packet with the flag

free(message); //free memory previously allocated for receiving the message

return packetSize; //return the packet size
transmitDataCC1020(packet : char *, length : int) : void. Transmit data to the modem.

Before using this method, it is necessary to set the SPI interface (setSPI-cc1020(): void) and configure the transceiver (configCC1020(): void and setTXmode(on : bool)).

\[
\text{for (int } i = 0; i < \text{length; } i++)\{
    \text{while (!uartA0.isTXready()); // wait until the TX buffer is ready}
    \text{uartA0.writeData(packet[i]);}
\}
\]

receiveDataCC1020(packet : char *) : int. Receives one packet and returns its length (in terms of number of bytes, excluding the two flags). Before using this method, it is necessary to set the SPI interface (setSPI-cc1020(): void) and configure the transceiver (configCC1020(): void and setRXmode(on : bool)).

\[
\text{char buffer;}
\]

\[
(BkIB31A1S_OBRF_437MHz$RX_structure *) tmp;
\]
bool first=true; //the head of the list has not been implemented yet

length=0;

while(!uartA0.isRXready()){ //wait until the buffer is ready to
    //be read
    buffer=uartA0.readData(); //read data from the buffer
    if(buffer==126)
        break; //starting flag has been identified
}

while(1){
    while(!uartA0.isRXready()){ //wait until the buffer is ready to
        //be read
        buffer=uartA0.readData(); //read data from the buffer as soon as
        possible
        if(buffer==126){
            tmp=head;
            packet=(char *) malloc(length*sizeof(char));
            if(packet==null)
                return 0; //error in malloc
            for(int j=0; j<length; j++){
                packet[j]=tmp->data;
            }
        }
    }
}
tmp=tmp->next;
}
free(head);
free(ptr);
return length; //final flag has been detected

if(first=true)

(Bk1B31A1S_OBRF_437MHz$RX_structure *)
head =
(Bk1B31A1S_OBRF_437MHz$RX_structure *) malloc(sizeof
(Bk1B31A1S_OBRF_437MHz$RX_structure)); //allocate a new

if (head==null)

return 0; //error in malloc
first=false;
head->data=buffer;
tmp=head;
else

(Bk1B31A1S_OBRF_437MHz$RX_structure *) ptr =
(Bk1B31A1S_OBRF_437MHz$RX_structure *) malloc(sizeof
(Bk1B31A1S_OBRF_437MHz$RX_structure)); //allocate a
if (ptr==null)
{
    return 0; // error in malloc

    ptr->data=buffer;
    tmp->next=ptr; // link the chain
    tmp=ptr;
    length++; // increment the length of the list
}

return 0; // in normal operations, the program will never reach this line

isRXpacketCorrect(packet : char *, length : int) : bool Returns true if the CRC check asserts the packet is correct. Returns false in the other way round. The packet under check is supposed to be received from receiveDataCC1020(packet : char *): int, so flags have been already removed.

% isRXpacketCorrect(packet : char *, length : int) : bool

if(crcByteWise(packet,length)==0)
{
    return true;
}
else
    return false;

sendDataOBC(message : char *, length : int) : void. Send data to OBC. Before using it, it is necessary to initialize the microcontroller and the SPI interface.

for (int i = 0; i < length; i++){
    while (!uartB2.isTXready()); // wait until the TX buffer is ready
    uartB2.writeData(message[i]);
}
This chapter is completely devoted to the antenna design and the microwave propagation issues. As a matter of fact, according to the system level design the radiating apparatus is the last block to be designed. Radio frequency attenuation, scattering and depolarization phenomena are firstly studied. Secondly, suitable on-board and ground station UHF antennas are analyzed in order to provide a background for the reader. Then, the linear polarized radiating systems are selected for the satellite application and both design and simulations are carried out. Loops, dipoles and monopoles are considered and different configurations (i.e. both standing alone and within the cubic AraMiS shape) are evaluated. As a conclusion, the best compromise in terms of mechanical constraints, electrical matching and radiation efficiency is going to be highlighted.

8.1 Microwave propagation

8.1.1 Clear-sky-induced propagation effects

Whenever the line of sight within the troposphere is free of obstructions (e.g. clouds, rain or other hydrometeors) the two main constituents are nitrogen (78.1%) and oxygen (20.9%). The proportions of these gases are fixed and their effects for any radio link are constant. In contrast, water vapor is characterized by varying proportions (within 4% near surface, lower than 0.01% above 15 Km) and such a change causes most of the clear-sky impairments[12].

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Although the microwave band ranges from 300 MHz to 300 GHz, water vapor and oxygen cause strong absorption of radio waves at frequencies above 1 GHz. Moreover, water vapor distribution and variation of density, temperature and pressure as a function of altitude contribute to the systematic ray bending. As a matter of fact, those create modifications to the radio refractive index. However, because of random local inhomogeneities, other impairments at microwave frequencies may arise, such as changes in angle of arrival, amplitude/phase fluctuations and phase delay. The longer the path through the atmosphere, the more severe these impairments tend to be. The situation is further complicated by the fact that the transmission properties of the atmosphere vary both diurnally and seasonally as well as geographically.

Antenna design is affected by absorption in the clear atmosphere \( (A_a) \), so a higher gain may be required to overcome such an issue. By defining a linear path length \( (d) \), the general absorption coefficient \( (\gamma_a, \left[\frac{\text{dB}}{\text{Km}}\right]) \), the absorption coefficient due to oxygen \( (\gamma_O, \left[\frac{\text{dB}}{\text{Km}}\right]) \), the absorption coefficient due to water vapor \( (\gamma_w, \left[\frac{\text{dB}}{\text{Km}}\right]) \), the water vapor concentration \( (\xi, \left[\frac{\text{g}}{\text{cm}^3}\right]) \) and the working frequency \( (f) \), the following relation holds.

\[
A_a = \int_{\text{path}} \gamma_a(r) dr = \gamma_a d = d [\gamma_O (f) + \gamma_w (f, \xi)]
\]

In ground-satellite communications, the elevation angle \( (\theta) \) is crucial because it determines the actual path length through the atmosphere and an approximate formula to easily compute the attenuation factor as a function of \( \theta \) is \( \gamma_a (\theta) \approx \frac{\gamma_a (90^\circ)}{\sin (\theta)} \) [12]. That is sufficiently accurate for down to 5° elevation angles.
Figure 133: Specific attenuation for water vapor and oxygen[12]
Beyond attenuation issues, ray bending is another effect which requires countermeasures. It arises because of the variation in the refraction index and, for lower elevation angles, an empirical exponential model is usually considered.

\[ n(h) = 1 + (77.6 \frac{p}{T} + 3.73 \cdot 10^5 \frac{p_w}{T^2}) \cdot 10^{-6} = 1 + 315 \cdot 10^{-6} \cdot e^{-0.136h} \]

Where, \( h \) is the altitude above sea level, \( p \) is the atmospheric pressure [mb], \( T \) is temperature [K], \( p_w \) is the water vapor pressure [mb].

Moreover, at any point of the ray path, the curvature is defined as the reciprocal of the radius (\( \rho \)) in the following way:

\[ \frac{1}{\rho} = \frac{\cos(\theta)}{n} \cdot \frac{dn(h)}{dh} \]

For Earth-space radio links, ray bending is in general downward and implies both the need of higher elevation angle for pointing the antenna and a reduction in the field-of-view of the satellite.

8.1.2 Rain-induced propagation effects

Rain is the major cause of impairments in the band of interest because of absorption and EM scattering. Firstly, those actions cause signal attenuation and produce polarization changes. Additionally, scattering diverts radio waves causing interference among telecommunication systems operating at the same frequency[12].

In order to estimate those impairments, it is necessary to know the local rainfall climate in terms of rate and drop-size distribution. Ideally, one would like to know the rainfall characteristics for many years and the experimental consequences connected to the radio links, but
this information is commonly not available. In contrast, designers use to take advantage from the parameters which are obtainable by global weather services, then they interpolate for the specific geographic area of interest.

Rain-induced attenuation \( A \) and depolarization are functions of the rain rate \( R \), the impairment per unit path length \( \gamma(R) \) and the effective path length through the medium \( L_e \). \( \gamma(R) \) is shown in Figure 134, while \( L_e \) is going to be described in the following.

\[
A = L_e(R, \theta)\gamma(R)
\]
Rain rate is never constant through the radio path, so the actual thickness of the atmospheric disturbance is not sufficient to compute the attenuation. Such a phenomenon has led to the concept of effective path length ($L_e$) and its formulation, based on empirical data collected in western Europe and North America, is exposed in Figure 135.

$$L_e(R, \theta) = \left[0.00741R^{0.766} + (0.232 - 0.00018R) \sin \theta\right]^{-1}$$

Unfortunately, not all raindrops are spherical since, when sizes are larger than 0.5 mm in radius, their shape evolves to either flattened spheroid (distorted by the air pressure when falling) or cardioids (when radius is greater than 3 mm). As a result, attenuation due to rain is polarization-sensitive because, when the ray transits through the raindrop in a perpendicular way with respect to its major axis, it results lower than the other way round. In general, most non-spherical raindrops fall with their major axis only slightly inclined to the horizontal. Thus,
considering a ground-satellite communication, a radio wave which is horizontally polarized is less attenuated than a vertically polarized one.

As a conclusion, rain effectively leads to power losses and a degradation of the system noise temperature. Those effects can be compensated by increasing the antenna gains, increasing the transmitted power and reducing the receiver noise temperature.

8.2 UHF radiating systems for point-to-point communications

8.2.1 Generalities

At the beginning of the thesis, the link budget has been computed by supposing two suitable parameters for the antenna gains. In order to have a rough estimation, just a simple dipole and a helix antenna have been assumed for the ground station and the satellite. For convenience, Table XXXVII points out the set of values which characterize the wireless communication link.

<table>
<thead>
<tr>
<th>$L$</th>
<th>$f$</th>
<th>$\lambda$</th>
<th>$\alpha_{att}$</th>
<th>$g_{dipole}$</th>
<th>$g_{helix}$</th>
<th>$P_{TX_{gnd}}$</th>
<th>$P_{TX_{sat}}$</th>
<th>$\chi$</th>
</tr>
</thead>
<tbody>
<tr>
<td>600 Km</td>
<td>437 MHz</td>
<td>68.65 cm</td>
<td>-154.3 dB</td>
<td>2 dB</td>
<td>15 dB</td>
<td>47 dBm</td>
<td>33 dBm</td>
<td>-3 dB</td>
</tr>
</tbody>
</table>

The goal is now to determine how to physically achieve suitable structures for matching those requirements. Firstly, due to mechanical reasons and the unavailability of free space, the gain distribution between satellites and ground stations cannot be symmetrical and it is always necessary to achieve as much gain as possible from the base station antenna. As a matter of
fact, the larger the antenna, the higher the gain, but the AraMiS telecommunication tile is very small.

Beyond gain issues, the choice of polarization is also crucial because it determines the shape associated to the radiating system. On the one hand, orthogonal linear polarizations are usually chosen in order to increase EMI isolation, but, on the other hand, circular polarization allows to reduce the destructive interference coming from reflected multipath signals. Additionally, circular polarization is often used whenever the TX/RX orientation cannot be easily controlled, such as in spacecraft communications.

In the following paragraphs a brief description of common antennas for point-to-point links is going to be depicted[9].

8.2.2 Yagi-Uda

These antennas are widely used at frequencies up to 2.5 GHz. They are cheap, quite simple to construct and provide gains of up to about 17 dBi (even more when a multiple array is used). At low frequency (down to 30 MHz) the gain is limited by the physical size of the antenna and, in the UHF band reflector systems are usually preferred because of their large gain availability.

A Yagi-Uda antenna consists of a single driven element and a set of parasitic ones (reflector and directors). The driven element is typically a \( \frac{\lambda}{2} \) dipole and it is the only metal structure which is directly excited (i.e. electrically connected to the feedline). All the other elements are considered parasitic because they just re-radiate the power received from the driven element and they interact with each other. The reflector is longer than the resonant wavelength, so its electrical behaviour is inductive and it reflects the electromagnetic wave coming from the
driven dipole in the opposite direction (i.e. toward the directors). The directors (up to 20) are shorter, so they show capacitive electrical behaviour and make the radiating system more directive along their direction. All the elements are usually parallel in one plane and supported by a single crossbar known as a boom.
As shown in the Figure 136, Yagi-Uda antennas provide a unidirectional beam with moderately low side and rear lobes[9]. In order to increase the back-to-front ratio up to 40 dB, an additional screen must be placed to the rear. Moreover, when individual antennas are correctly spaced, an array of N antennas can roughly provide a power gain which is N times larger.

Regarding polarization, a standard Yagi-Uda antenna provides linear polarization since that is determined by the fed dipole.
8.2.3 Helices

A helical antenna consists of a conducting wire wound in the form of a helix. In most cases, helical antennas are mounted over a ground plane and the feed line is connected between the bottom of the helix and the ground plane.

Those systems can operate either in normal or axial mode. When operating in normal mode, the antenna is also known as a broadside helix and the dimensions (including the diameter and the pitch) are electrically small. In this case, the antenna acts as an electrically short dipole: the radiation pattern is omnidirectional, the maximum radiation is at right angles to the helix axis and polarization is linear. Such a system is adopted in portable radios, but it is useless in satellite communication since high gain is expected.
In contrast, the axial mode leads to the so-called end-fire helix and takes place when the dimensions are comparable to the wavelength. In this case, the system works as a directional antenna, the main beam stands along the helix axis and EM fields are now circularly polarized[9]. The maximum gain typically ranges from 12 dBi at 150 MHz to 20 dBi at 2 GHz and it is limited by the physical length of the antenna.

8.2.4 Panel antennas and paraboloids

Any radiating system which includes a reflecting screen and simple radiating elements mounted in a broadside configuration is generally called panel antenna[9]. An array may also contain one or more panels connected together in order to increase the overall gain. Typical configurations use full-wavelength dipoles, half-wave dipoles or slots as radiating elements and they have several advantages with respect to Yagi-Uda antennas:

- more constant gain, radiation patterns and VSWR over a wider bandwidth (up to an octave);
- more compact physical construction;
• very low coupling to the mounting structure;

• lower side lobes and rear lobes.

In case of paraboloids, the reflecting screen is called aperture and its size is only determined by the required gain, independently from the feed nature. The design requires to select the reflector size and specify the radiation pattern concerning the illuminating antenna. If the antenna aperture is incompletely filled or its illumination is nonuniform, the corresponding gain decreases. Regarding this, the ratio between the achieved gain to the maximum available one is termed the *aperture efficiency* ($\epsilon_{so}$).

In the UHF band, a reflector can be made of a solid sheet, a perforated sheet or a set of parallel curved rods. In Table XXXIX, a set of typical configurations is shown, where $D$ is the aperture dish diameter and $F$ is the focal length.
Grid paraboloids are widespread because the curvature associated to the rods is exactly the same, while just their length varies across the antenna. Such a structure is characterized by an easy physical implementation, a low weight structure and a low wind-loaded area, while the main drawback is given by the power leakage through the surface. In contrast, metal sheets are used when the power leakage must be minimized.

8.3 Satellite antennas

8.3.1 Radiation pattern and mechanical stability

A spacecraft can derive its mechanical stability (i.e. the attitude control) by means of different actuators. Firstly, the conservation of angular momentum allows to orientate the satellite through the gyroscopic action produced by rotating a mass (e.g. reaction wheel).
Additionally, magnetic actuators could be added to generate magnetic fields and they produce a mechanical torque as a result of the interaction with the Earth’s magnetosphere.

Basically, the antenna design is strongly conditioned by the degree of mechanical stability associated to the spacecraft. For instance, when the satellite is two-axis stabilized (e.g. only magnetic actuators are used) there is just a planar control. That means the system can be oriented along a specific axis without any control on the random rotation around it. In contrast, the three-axis control (e.g. at least two reaction wheels are used) allows to fully stabilize the spacecraft and all the spinning rotations are canceled.

Regarding this, a two-axis stabilization requires the radiation pattern to be omnidirectional over the plane perpendicular to the axis of rotation[10]. As a matter of fact, in such a situation the spinning becomes transparent to the ground station and the radio link is not affected when circular polarization is used at least by one node. Alternatively, the antenna must be designed so that its radiation pattern is electrically (i.e. antenna arrays) or mechanically adjustable. In fact, it is necessary to ensure the main beam along the direction of interest and the correct polarization alignment. For example, if linear polarization is used by both TX and RX, a two-axis control is sufficient to ensure that the main beams coincide, but, in case of rotation around the line of sight, the communication stops working every time there is a strong polarization mismatch.

8.3.2 Polarization

In this subsection there is a review of the most important features concerning the polarization choice in the satellite background.
For example, *linearly polarized antennas* are characterized by the rejection of the orthogonally polarized waves. As previously mentioned, such a behaviour is useful to reduce EM interference when orthogonal polarizations are selected for different radio links. In contrast, that phenomenon creates depolarization losses when, although the planes containing the TX/RX antennas are parallel, the two metal structures are reciprocally rotated (e.g. just two-axis control is available).

Secondly, *circularly polarized antennas* are orthogonal when the associated EM fields rotations are reverse. As a matter of fact, the right-hand rotation implies that the electric field vector rotates in a clockwise sense as the wave is propagating away from the observer, while the left-hand rotation implies the other way round. In this context, any rotation of the radiating system over its plane does not affect the wave polarization, so that is suitable for two-axis stabilized satellites.

Moreover, the orientation associated to the linearly polarized waves is altered by the Earth’s ionosphere due to the *Faraday rotation effect*. Such a phenomenon is not negligible at frequencies lower than 1 GHz, so it is going to be considered in the AraMiS design.

This effect leads to a phase shift ($\beta$) of the EM phasors ($E$ and $H$) and that is due to the interaction between the static magnetic flux density along the direction of propagation ($B$) and the medium. Calling $\nu$ the Verdet constant and $d$ the path thickness, the following relation holds\[12\]:

$$\beta = \nu dB \propto \frac{1}{f^2}$$
Another advantage of using circularly polarized waves is that they are almost immune from the Faraday rotation effect.

### 8.3.3 Earth-coverage antennas

The most common satellite antennas have a broad pattern which has an approximately constant gain over the portion of Earth they can view from space. These are called *Earth-coverage antennas* and vary from simple dipole arrays to horn antennas or reflectors. For LEO satellites like AraMiS, the maximum angle subtending the Earth ($\theta_0$) is relatively large, so the associated radiating system may be just a single dipole, a loop or a helix. In contrast, higher-altitude satellites usually adopt horn type antennas because they are more directive (Figure 141).
\[
\theta_0 = \sin^{-1}\left(\frac{R}{R+h}\right)
\]

At frequencies lower than 1 GHz, atmospheric attenuation is negligible and the power that is actually received on the Earth’s surface is basically a function of the path length \(t\). However, at frequencies above 10 GHz, atmospheric attenuation becomes significant especially due to water-vapor, oxygen molecules and raindrops (up to 3 dB at 45 GHz). In this case, as a first order approximation the total attenuation \(A\) is proportional to the path length \(L_a\) through the atmosphere[10]. In Figure 142, there is a graphical representation of the satellite scenario, where \(h_a\) is the atmosphere thickness (approximately constant) and \(\phi\) is the elevation angle.

The desired Earth-coverage antenna pattern \(d(\theta)\) must compensate the change of \(t(\theta)\) and \(A(\theta)\) over the entire field of view, so it is expected an optimal radiation pattern having the following form:
In order to determine $A(\theta)$, it is firstly necessary to compute $L_a$ as follows:

$$
L_a = \left[(R + h_a)^2 + R^2 - 2R(R + h_a)\cos\alpha\right]^{\frac{1}{2}} 
\approx h_a \left[1 + 4\left(\frac{R}{h_a}\right)^2 \sin^2\left(\frac{\alpha}{2}\right)\right]^{\frac{1}{2}}
$$

where $\frac{R}{h_a} \gg 1$ and $\alpha \approx \frac{\pi}{2} - \phi - \sin^{-1}(\cos\phi)$.

Hence, $A(\theta) = e^{A_0\left(1 - \frac{L_a}{h_a}\right)}$ where $A_0$ is the attenuation when $\phi = \frac{\pi}{2}$.

In order to compute $t(\theta)$, it is convenient to define the angle $\beta = \frac{\pi}{2} - \theta - \phi$, where $\phi = \cos^{-1}\left[(1 + \frac{h}{R})\sin\theta\right]$. As a matter of fact:

$$
t(\theta) = h \left\{R^2 + (R + h)^2 - 2R(R + h)\cos\beta\right\}^{\frac{1}{2}}
$$

The antenna maximum directivity can be computed starting from the general form, then considering the omnidirectional radiation with respect to the $\varphi$-angle:
\[ D = \int_{\Sigma} \int_{\Omega} d(\theta, \varphi) \sin(\theta) d\theta d\varphi = \frac{2}{\int_{0}^{\theta_1} d(\theta) \sin \theta d\theta} \]

\[ \theta_1 = \sin^{-1} \left( \frac{R \cos \phi_0}{R+h} \right) \]

where \( \theta_1 \) is the coverage area edge, \( \phi_0 \) is the minimum safe satellite elevation angle (usually \( 10^\circ \)) and \( d(\theta) = 0 \) whenever \( \theta > \theta_1 \).

In the case of synchronous orbit (geostationary orbit) satellites, the theoretical maximum directivity of an Earth coverage antenna is about 24 dB.

The following MATLAB script computes the maximum directivity, the field of view and the radiation pattern for the AraMiS LEO target.

```matlab
% Maximum Directivity, FOV and Radiation Pattern for %
% a possible Earth-coverage AraMiS Application %

clear all
close all
clc

h=600; % altitude of the satellite [Km]
A0=0.5; % Zenit atmospheric attenuation [dB]
R=6378; % Earth radius [Km]
```
\[ \text{phi}0 = 10; \] % minimum suitable elevation angle of the satellite [deg]

\[ \text{ha} = 100; \] % thickness of the relevant atmosphere [Km]

\[ A_{\text{lin}} = 10^{(A0/10)}; \]

\[ A_{\text{lin}} = 0; \] % since the working frequency is 437 MHz

\[
\text{phi0rad} = \text{phi0} * \pi / 180;
\]

\[
\text{tmpfunc} = \text{inline}'(h.*(1+4.*((R./h).^2+R./h)*sin((pi./2-theta-(acos((1+h./R)*sin(theta))))./2).^2).^0.5.*h^2', 'h', 'R', 'theta');
\]

\[
\text{FOV} = \text{asin}(R/(R+ha)); \] % Field of view

\[
\text{thetaPoints} = \text{linspace}(0, \text{FOV}, 1000);
\]

\[
\text{gamma} = 1/\text{max}((\text{tmpfunc}(h,R,\text{thetaPoints})));
\]

\[
\text{integrando} = \text{inline}'(\text{gamma}.*(h.*(1+4.*((R./h).^2+R./h)*sin((theta)))./2).^2).^0.5.*h^2.*exp(A_{\text{lin}}*(1*)((R+ha).^2-2.*R.*(R+ha).*cos(pi/2-acos((1+h./R).*sin(theta)))-asin(acos((1+h/R).*sin(theta))).^0.5./ha))./h^2.*sin(theta)', 'gamma', 'h', 'R', 'A_{\text{lin}}', 'ha', 'theta');
\]

\[
\text{integral} = \text{quad}(\text{integrando}(\text{gamma},h,R,A_{\text{lin}},ha,\text{theta}),0,\text{phi0rad});
\]

\[ D = 2/\text{integral}; \]
\[
\text{plot} \left( \text{thetaPoints*180/pi}, 10*\log10\left( \text{tmpfunc(h,R,thetaPoints)*gamma*D} \right) \right); \\
10*\log10(D)
\]

Assuming the altitude of the satellite equal to 600 Km, the UHF working frequency and a minimum elevation angle equal to 10°, the field of view is approximately 66°, while the directivity for the Earth-coverage antenna ranges from 21 dB to 35 dB.

![Required radiation pattern (MATLAB)](image)

Previous results point out that the Earth coverage is not feasible for the AraMiS architecture because the maximum directivity is too high for such a low cost and low mass satellite.

### 8.3.4 Spot-beam coverage

In contrast with the Earth coverage radiating systems, spot-beam coverage consists in providing a higher gain pattern for serving a very smaller region. As a consequence, in order to
cover the complete field of view (FOV), it is necessary to split the Earth surface in different cells and sequentially scan among them[10]. That is performed by means of either mechanical or electronic steering. The minimum directivity within a single cell allows to estimate the worst case system performance and that is what is going to be computed in this subsection.

Since the cross section of a high gain beam is usually circular, the following analysis considers $N$ beams having a circular cross section. Then, they are arranged over a triangular grid with a beam-axis-to-beam-axis angular separation equal to $\theta_b$. When referring to such a scenario, in order to simplify calculations it is usual to indicate each beam by a uniquely defined hexagonal area, as shown in Figure 144.

![Figure 144: Spot-beam coverage[10]](image)
Taking advantage from such a regular geometry, the analysis just considers the brown area depicted in the picture, then a Gaussian-shaped beam is assumed. The goal is to determine $\theta_b$ and the beam directivity $D_0$ which maximizes the minimum directivity ($D_m$) (i.e. the directivity on the cell borderline).

According to the previous assumptions, the generic beam directivity is represented by the following function:

$$D = D_0 e^{-\alpha \left(\frac{2\theta}{\theta_1}\right)^2}$$

where, $\theta_1$ is the half-power beamwidth associated to each beam and $D_0 = \eta \frac{4\pi}{\theta_1^2}$, with $\eta [0.5, 0.8]$. Since $D = \frac{D_0}{2}$, when $\theta = \frac{\theta_1}{2}$ it is possible to compute $\alpha = \ln (2)$. Hence,

$$D = D_0 e^{-2.77 \left(\frac{\theta}{\theta_1}\right)^2} = D_0 e^{-0.22\theta^2 \frac{D_0}{\eta}}$$

As shown in Figure 144, $D_m$ occurs in the middle of the equilateral triangle formed by the center-points of any three adjacent cells. Then, the angle $\theta_m$ between the axis of any beam and the direction of minimum gain is given by $\theta_m = \frac{\theta_b}{\sqrt{3}}$. Hence,

$$D_m = D_0 e^{-0.0746^2 \frac{D_0}{\eta}} = D_0 e^{-BD_0}$$

Differentiating $D_m$ with respect to $D_0$ gives $\frac{\partial D_m}{\partial D_0} = (1 - BD_0) e^{-BD_0}$, where $B = \frac{0.0746^2}{\eta}$. As a result, $D_m$ is maximized when:

$$D_0 = \frac{\eta}{0.0746^2}$$

So the maximum value for $D_m$ is equal to $D_{max} = D_0 e^{-1} = D_0 (dB) - 4.34dB$. 

As a conclusion, the best spot-beam coverage design must be carried out in the following way:

- the first step is to choose the antenna having maximum available gain ($D_0$);
- since $D_0 = \frac{\eta}{0.0746}$, it is possible to compute $\theta_b$ by inverting the equation;
- the number of cells ($N$) which maximize the worst case directivity is geometrically deduced;
- the worst case directivity is $D_0 - 4.34$ dB and takes place among three adjacent beams;
- the directivity between two adjacent beams is $D_0 - 3.24$ dB.

In order to simplify the mechanical structure and to compensate for a low cost attitude control system, the helix antenna will not be considered for the AraMiS purposes. In contrast, just low gain antennas such as loops and dipoles are going to be analyzed (see next chapters). Then, since $D_0$ would be around $2$ dB, previous results point out that spot beam coverage is not feasible because the worst case directivity would be too low for an acceptable design (lower than $0$ dB).

8.4 Earth station antennas

8.4.1 Introduction and general characteristics

The main electrical specifications associated to a ground station antenna are basically gain, noise temperature, VSWR, power rating, RX/TX group delay, radiation pattern, polarization and isolation. Although almost all the parameters are only determined by system requirements, the radiation pattern must also meet some constraints defined by both ITU-R (international agreements) and the national laws.
Depending on the electrical size associated to the antenna ($D$ is the maximum physical dimension), the standard basically specifies the following reference envelope for sidelobes[11].

$$G = \begin{cases} 
[49 - 10 \log \left( \frac{D}{\lambda} \right) - 25 \log \theta] \text{ dBi} & D \leq 100 \lambda \\
(29 - 25 \log \theta) \text{ dBi} & D > 100 \lambda 
\end{cases}$$

In general, Earth station antennas can be grouped into two categories: \textit{single-beam antennas} and \textit{multiple-beam ones}. The former typology consists of radiating systems which generate a single beam for pointing a single satellite through specific positioning systems. In contrast, the latter set of antennas is associated to a multiple beam generation by means of a common reflector having multiple feeds. Such a structure allows to simultaneously manage several satellites.

In the following subsections, a brief description of the basic structures is carried out.

8.4.2 \textbf{Single-beam antennas}

8.4.2.1 \textbf{Dual-reflector antennas}

Nowadays, the predominant design choice for Earth stations is the \textit{dual-reflector Cassegrain antenna}. This approach is an alternative to the common paraboloidal antenna design, where the feed is mounted in the dish focus. As a matter of fact, the Cassegrain design shows several advantages which can justify its increased complexity:

- the feed (i.e. waveguides and the front-end electronics) can be located either over or behind the dish, rather than suspended in front where it would block part of the emitted beam;
• since the feed antenna is forward directed, the TX spillover sidelobes caused by portions of the beam which miss the secondary reflector are upward directed (i.e. toward the sky). In contrast, the paraboloidal structure was based on a backward oriented feed which produced sidelobes toward Earth\[11\]. In RX mode, such a precaution reduces the reception of ground noise;

• Cassegrain design also increases the focal length associated to the antenna and that allows to make narrower the field of view.

The classical Cassegrain geometry has a paraboloidal contour acting as main reflector and a hyperboloidal one for the subreflector. The paraboloidal reflector is a point-focus device with diameter $D_p$ and focal length $f_p$, while the subreflector has two foci. One of the two foci is the real system focal point and is located in order to coincide with the feed phase center, that is the apparent antenna center where spherical waves are supposed to be emanated from. In contrast, the other focus is the virtual focal point and is located in order to coincide with the main reflector focal point. In a typical design, $f_p$, $D_p$, $f_s$ and $\phi_s$ are chosen, while the other parameters shown in Figure 145 are consequently computed.
8.4.2.2 Offset-fed reflector antennas

The offset-fed reflector consists of a paraboloidal section instead of a complete surface. The main advantage is that there is no more any field blockage by the feed supporting structure.

\[
\begin{align*}
\phi_p &= 2\tan^{-1}\left(0.25 \frac{D_p}{F_p}\right) \\
\frac{L_s}{d_s} &= 0.5 \left(\cot\phi_p + \cot\phi_s\right) \\
\frac{L_s}{f_s} &= 0.5 \left(1 - \frac{\sin(0.5(\phi_p - \phi_s))}{\sin(0.5(\phi_p + \phi_s))}\right)
\end{align*}
\]
In this context, sidelobe levels are usually upper bounded by the following relation[11]:

\[ f(\theta) = (29 - 25\log\theta) \text{ dBi} \]

where \( \theta \) is the far-field angle in degrees. Moreover, offset-fed reflector antennas show higher aperture efficiency with respect to the common paraboloids, since it ranges from 65% to 80%. The disadvantage associated to such a structure is that it is asymmetric, so manufacturing cost is higher and there are some negative effects on the electrical performance. For instance, a significant depolarizing effect takes place when linear polarization feed is used. As a matter of fact, in such a situation two cross-polarized lobes arise very close to the main beam. Additionally,
when offset-fed reflector antennas are used with circular polarization, a small amount of beam squint is introduced according to the following relation:

$$\psi_s = \sin^{-1}\left(\frac{\lambda \sin \theta_0}{4\pi F}\right)$$

where, $\theta_0$ is the offset angle, $\lambda$ is the free-space wavelength and $F$ is the focal length.

### 8.4.3 Multiple-beam antennas

#### 8.4.3.1 Spherical reflectors

Among the multiple-beam antennas, spherical reflectors are probably the most widespread ones. That is primarily due to the ease of physical implementation with respect to the paraboloidal structures. Moreover, the circular symmetry allows to simplify multiple-beam operations by placing all the feeds along the same surface (Figure 147).

![Figure 147: Conventional spherical multi-beam antenna using multiple feeds][11]
Each individual feed illuminates a portion of the reflecting surface, then a reflected beam is generated in the opposite direction[11]. All beams have similar radiation patterns and gains, but there is degradation in performance with respect to paraboloids. The advantage of spherical reflectors is that the reflecting area illuminated by each individual feed can overlap, so the aperture area can be optimized.

8.4.3.2 **Torus antennas**

The torus antenna is a *dual-curvature reflector* which allows multi-beam operations. The reflector has a circular contour in the yz-plane and a paraboloidal one in the xz-plane (Figure 148).

![Torus-antenna geometry](image-url)
The presence of two different contours allows to take advantage from both geometries[11]. As a matter of fact, the paraboloidal shape ensures the offset-fed capability (i.e. the unblocked aperture increases the radiation performance), while the circular contour allows a better surface optimization (i.e. reflecting areas can overlap). Moreover, due to the presence of focal points, the torus radiating systems show a lower phase aberration with respect to spherical antennas. Finally, the circular symmetry also allows identical reflected beams when feeds are placed on the same arc.

8.4.4 Ground station at Polytechnic of Turin

The ground station at Polytechnic of Turin is a satellite radio communication system which works at different frequency ranges. The ground station is both HW and SW compatible with the GENSO architecture and there are two separate antenna systems, one for the VHF/UHF frequencies and the other for the S-band (2.4 GHz). Moreover, a single rack contains the electronic and radio communication equipment, while a PC is used as a station controller and GENSO node.
Figure 149: Antennas at Polytechnic of Turin

TABLE XL: SPECIFICATIONS OF THE GROUND STATION AT POLYTECHNIC OF TURIN

<table>
<thead>
<tr>
<th>Band</th>
<th>Structure</th>
<th>TX power [W]</th>
<th>Polarization</th>
<th>Gain [dBi]</th>
</tr>
</thead>
<tbody>
<tr>
<td>VHF</td>
<td>2 crossed Yagi (10+10 el.)</td>
<td>100</td>
<td>RHCP</td>
<td>17</td>
</tr>
<tr>
<td>UHF</td>
<td>4 crossed Yagi (18+18 el.)</td>
<td>70</td>
<td>RHCP</td>
<td>22</td>
</tr>
<tr>
<td>S</td>
<td>$D = 3 \text{ m} - \frac{F}{D} = 0.3$ paraboloidal reflector</td>
<td>25</td>
<td>RHCP</td>
<td>33</td>
</tr>
</tbody>
</table>
In order to ensure the satellite tracking, two variable speed DC-motors are used to achieve a 0.5° resolution.

Table XL shows that the ground station is also coherent with the electronic design developed in this thesis. As a matter of fact, both the transmitted power and the gain associated to the UHF channel are even greater than the values which were assumed.

8.5 Loop-antenna design

8.5.1 AraMiS context

All previous considerations regarding polarization issues would apparently lead to the design of an on-board helix antenna because it allows circular polarization.

However, it must be taken into account that generally small and low-cost university satellites should keep a regular shape. That is required in order to be compatible with the free available space left by main payloads inside the launcher. Such a requirement conflicts with a possible helix antenna because it would necessarily lead to an irregular protrusion for each telecommunication tile. Additionally, any elongated structure represents a possible hazard from the mechanical point of view due to both vibrations and dangerous interactions with other spacecrafts, especially during deployment.

Regarding the electrical features, it is not always convenient to perfectly align the on-board antenna with the ground station since such an operation is both power and time consuming. As a matter of fact, the visibility time is not so long for LEO satellites (approximately 10 minutes), so the need of additional time for the attitude control cannot be neglected. Moreover, it would be nice to maintain the telecommunication link even if the spacecraft is not pointing toward
the ground station because this eventuality may happen while the payload is working (e.g., a camera is taking pictures somewhere else). Finally, an accurate attitude control system can be expensive and a perfect alignment with the RX antenna can be difficult for a low cost system.

By taking advantage from the ground station which is characterized by a relative high-gain, high TX power and tracking capability, it is possible to design the on-board antenna with low directivity. That allows the satellite to communicate even if its orientation is not accurate and the power dispersion resulting from a non-directive pattern would be compensated by the ground station. For instance, the CubeSat standard for UHF/VHF communications includes a simple dipole which extend only after the satellite deployment. Such a radiating system is associated to the linear polarization, so on the one hand it is expected both depolarization loss and a stronger attenuation in the troposphere, but on the other side the mechanical structure becomes more regular.

Similarly, in the following section a loop-antenna design is carried out since it provides a broad radiation pattern and minimizes the required space for the metal structure. Additionally, the loop does not require any extension procedure after deployment, so it is even more reliable. In this context, the single-turn loop antenna consists of a metallic conductor bent to make a closed curve (e.g., a circle or a square). Then, the contour must be cut in order to origin a small gap for the two terminals. In order to be also compatible with the CubeSat standard, a loop having diameter equal to 9 cm and thickness lower than 1 cm is taken as an upper-bound.

The following symbols are used throughout the design:

- \( \lambda \approx \frac{c}{f} \approx 68.6 \text{ cm} \) is the free-space wavelength at frequency \( f = \frac{\omega}{2\pi} \approx 437 \text{ MHz} \);
• $\beta = \frac{2\pi}{\lambda}$ is the propagation constant in free space;

• $\zeta = \sqrt{\mu_0/\epsilon_0} \approx 377 \, \Omega$ is the free space impedance;

• $b$ is either the mean radius of a circular loop or the half-side length associated to a square loop;

• $a$ is either the radius of a circular conductor or the half-side length associated to a square cross section. Anyway, $a$ is supposed to be much smaller than $b$;

• $A$ is the loop area;

• $N$ is the number of turns;

• $l_c$ is the length associated to the solenoidal coil;

• $p$ is the loop perimeter;

• $\frac{p}{\lambda} = 0.1 \rightarrow b_{\text{circle}} \approx 1.1 \, \text{cm}, b_{\text{square}} \approx 1.72 \, \text{cm}$ is the boundary condition between small and large loop approximation.

8.5.2 Electrically small loop

When $\frac{p}{\lambda} \leq 0.1$, the radiating system is an electrically small loop and this case is the most frequently encountered in practical applications, especially for portable radios and mobile phones.

Under this condition, the current distribution is assumed to be uniform ($I_0$) at any point of the conductor and the antenna is simply analyzed as a radiating inductor[5].

The electromagnetic fields of an electrically small loop antenna are equal to those of a magnetic dipole having moment $m = I_0NA$. They are described by the following equations:
Figure 150: Spherical coordinate system and the loop antenna[5]

\[
\begin{align*}
E_\phi &= \frac{\varepsilon_0 \beta^2 m}{4\pi r} \left( 1 - \frac{j}{\beta r} \right) e^{-j\beta r \sin \theta} \\
B_\theta &= -\frac{\mu_0 \beta^2 m}{4\pi r} \left( 1 - \frac{j}{\beta r} - \frac{1}{\beta^2 r^2} \right) e^{-j\beta r \sin \theta} \\
B_r &= \frac{\mu_0 \beta^2 m}{2\pi r} \left( \frac{j}{\beta r} + \frac{1}{\beta^2 r^2} \right) e^{-j\beta r \cos \theta}
\end{align*}
\]

where the loop antenna is considered within the coordinates system \((r, \theta, \phi)\) shown in Figure 150[13].

In far field condition, \(r\) is sufficiently large so that \(B_r\) becomes negligible. The vertical-plane field pattern associated to the relevant fields (\(|E_\phi|\) and \(|B_\theta|\)) is shown in the Figure 151. It is symmetrical with respect to the \(z\)-axis and omnidirectional over the \(xy\)-plane.

The driving voltage and current are related through the loop input impedance \((V = ZI_0)\), where \(Z\) depends on the series combination of the external inductance \(L^e\), the radiation resistance \(R^r\) and the internal impedance associated to the conductor \((Z^i = R^i + j\omega L^i)[5]\).
The external inductance is determined according to the winding density. For single-turn loops, $L^e$ is given by [5]:

$$L_{\text{circle}}^e = \mu_0 b \left[ \ln \frac{8b}{a} - 2 \right]$$

$$L_{\text{square}}^e = \frac{2\mu_0 b}{\pi} \left[ \ln \frac{b}{a} - 0.774 \right]$$

While, for a tightly wound solenoidal coil of length $l_c$ and radius $b$, $L^e = K\mu_0 N^2 A/l_c$. In the latter formula, $K$ is the Nagaoka’s constant and its value is shown in Figure 152.
Regarding the antenna equivalent circuit, a lumped capacitance $C_r$ is usually placed in parallel with $Z$ in order to make resonant the radiating system.

\[
\begin{align*}
L_{\text{tot}} & = L^r + L^i \\
R_{\text{tot}} & = R^r + R^i \\
C_r & = \frac{1}{2} \frac{L_{\text{tot}}}{L_{\text{tot}} + R_{\text{tot}}} 
\end{align*}
\]

As a result, the antenna input impedance becomes $Z_{\text{in}} = R_{\text{tot}} + \frac{L_{\text{tot}}^2}{R_{\text{tot}}}$. 

Figure 152: Nagaoka’s constant[9]
Additionally, for an electrically small loop the radiated power is given by

\[ P_{rad} = \zeta \frac{\pi}{12} (\omega \sqrt{\mu \epsilon b})^4 |I_0|^2 \]

and the directivity is approximately 1.76 dB[5].

In RX mode, the voltage at the open-circuited terminals (\(V_{OC}\)) is given by the following equation:

\[ V_{OC} = j\omega NAB_z^i \]

where \(B_z^i = B^i \cos \psi \sin \theta \) and the incident field \(B^i\) is assumed to be uniform over the small loop area (Figure 154).
$V_{OC}$ can be increased by filling the loop with a core permeable material (e.g. ferrite) because it would increase the magnetic flux through the loop area. Regarding this, the cylinder-core length ($l_r$) is assumed to be small compared to the wavelength in order to prevent internal resonances and losses (Figure 155).

$$l_r \ll \frac{\lambda}{\sqrt{\varepsilon_r \Re[\mu_r]}}$$

As a result, the open-circuit voltage ($V_{OC}$) is enlarged by the factor $\mu_{rod}$.\[5\]
An additional factor (called either $F_V$, $F_L$ or $F_R$ according to the formula where it is employed) must be included in order to take into account that the magnetic flux decreases along the coil length, starting from its maximum value in the middle[5].
Then, the presence of a permeable material produces an additional resistance ($R_m$) due to the core losses.

Finally, the following equations resume the behaviour of a core-loaded coil with $N$ turns.

\[
\begin{align*}
R_r &= \frac{\xi}{6}\beta^4 (\mu_{rod} F_V N A)^2 \\
R_m &= \omega \left( \frac{\mu_{rod}}{Re[\mu_r]} \right)^2 Im[-\mu_r] \mu_0 F_R N^2 A L_c \\
L^e &= \mu_{rod} F_L \mu_0 N^2 A L_c
\end{align*}
\]

A last remark concerns the overall antenna efficiency ($\eta$) because it accounts both conduction-dielectric losses ($R_{losses}$) and the reflection coefficient associated to the circuit.

\[
\eta = \frac{R_r}{R_r + R_{losses}} \left( 1 - |\Gamma|^2 \right)
\]

Since the presence of a ferrite core would introduce an interaction with the attitude-and-orbit-control-system (i.e. at least an offset would be added to the magnetic sensors), just a
stand-alone electrically-small single-loop antenna is assumed as a starting point for the AraMiS application. It must be also considered that in space applications the working temperature is highly variable, so the metal conductor must keep the intrinsic resistivity ($\rho(T)$) as much constant as possible (i.e. in the following equation $\alpha \to 0$).

$$\rho(T) = \rho_0 [1 + \alpha \Delta T]$$

A suitable material is titanium because it ensures an overall resistance variation within $3 \, \Omega$.

~~~

% Design of a stand-alone, electrically-small, %
% single-loop antenna made of Titanium and having %
% 50ohms as input impedance %
% (circular loop with circular cross section) %

clear all
close all
clc

loopRadius=1.1; %loop radius [cm]
conductorRadius=0.0135; %conductor radius [mm]
freq=437; %frequency [MHz]
\[\text{\texttt{zeta} = 377; \% free space impedance [Ohm]}\]
\[\text{c} = 3 \times 10^8; \% speed of light [m/s]\]
\[\text{\texttt{rho} = 4.2 \times 10^{-7}; \% metal resistivity (titanium)}\]
\[\text{\texttt{mu0} = 4 \times \pi \times 10^{-7}};\]

\[
f = \text{freq} \times 10^6;\]
\[
pul = 2 \times \pi \times f;\]
\[
\text{\texttt{lambda} = c / f;}\]
\[
\text{\texttt{b} = loopRadius / 100;}\]
\[
\text{\texttt{a = conductorRadius / 1000};}\]
\[
\text{\texttt{R1} = zeta / 6 / \pi * (2* \pi / lambda) \times 4 * (pi * b^2) \times 2;}\]
\[
\text{\texttt{R2} = rho \times 2 * b / (a^2);}\]

\[
\text{\texttt{Rtot} = R1 + R2}\]

\[
\text{\texttt{Le} = mu0 * b * (log (8 * b / a) - 2);}\]
\[
\text{\texttt{Li} = b / a * sqrt (mu0 / (2 * pul / rho));}\]

\[
\text{\texttt{Lt tot} = Le + Li}\]
\[
\text{\texttt{Cr} = Lt tot / (Rtot^2 +Lt tot^2) / pul}\]
\[
\text{\texttt{Zin} = Rtot + Lt tot^2 / Rtot}\]
In order to achieve the electrical matching, the antenna input impedance must be 50 Ω because that is the specification for both RX-input of the transceiver and the TX-output of the power amplifier. The last MATLAB script allows to find the set of parameters which fully matches those requirements.

**TABLE XLI: ELECTRICALLY SMALL CIRCULAR LOOP-ANTENNA DESIGN WITH 50Ω INPUT IMPEDANCE**

<table>
<thead>
<tr>
<th>Type</th>
<th>Value/Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R^r$</td>
<td>0.02 Ω</td>
</tr>
<tr>
<td>$\eta$</td>
<td>&lt; 5%</td>
</tr>
<tr>
<td>$Z_{in}$ (with $C_r$)</td>
<td>50.7 Ω</td>
</tr>
<tr>
<td>$L_{tot}$</td>
<td>101.7 nH</td>
</tr>
<tr>
<td>$C_r$</td>
<td>$1.44 \cdot 10^{-20} F$</td>
</tr>
<tr>
<td>$b$</td>
<td>1.1 cm</td>
</tr>
<tr>
<td>$a$</td>
<td>13.5 μm</td>
</tr>
<tr>
<td>Metal conductor</td>
<td>Titanium</td>
</tr>
<tr>
<td>$\rho_0$</td>
<td>$4.2 \cdot 10^{-7} \Omega \cdot m$ at 20 °C</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>$&lt; 10^{-5} K^{-1}$</td>
</tr>
</tbody>
</table>
Table XLI points out that the radiating resistance is very low (much lower than $1 \, \Omega$) and the electrical matching is not feasible due to the very low capacitance ($C_r$) which is required. Moreover, the thickness of the conductor results too low to be feasible, then a new material is considered. In case of nichrome ($\rho_0 = 1.10 \cdot 10^{-6} \, \Omega \cdot \text{m}$), the robustness is almost preserved, but the required thickness is now acceptable ($b \approx 25 \, \mu\text{m}$). However, the antenna efficiency is still low because the radiating resistance is much smaller than the ohmic trend associated to the metal conductor (i.e. the great majority of the electrical power would be wasted due to Joule effect).

Instead of enforcing $\text{Re} \left[ Z_{in} \right] = 50 \, \Omega$ (i.e. $RL = 0$), it could be possible to find a set of parameters which does not maximize the electrical matching, but ensures both higher radiation efficiency and feasible dimensions for the metal conductor. Regarding this, the return loss ($RL$) is considered acceptable as far as it is lower than $-10 \, \text{dB}$.

$$RL = 10\log_{10} \left| \frac{Z_{in} - 50\Omega}{Z_{in} + 50\Omega} \right|^2 \leq -10 \, \text{dB}$$

However, even by varying the loop radius and the conductor cross section, the main requirements are not met. As a matter of fact, keeping $RL < -10 \, \text{dB}$ still leads to low $C_r$ and insufficient antenna efficiency.

The first step in order to increase the antenna efficiency is to change material at the expense of mechanical and chemical performance, so copper is the new selected metal because of its easy availability and low resistivity ($1.69 \cdot 10^{-8} \, \Omega \cdot \text{m}$).

The next step is to consider a multiple-turns loop antenna for a further increasing of the antenna efficiency. Regarding this, the total ohmic resistance for an $N$-turns circular loop
antenna is \( R^i = \frac{N\mu}{a} R_s \left( \frac{R_p}{R_0} + 1 \right) \), where \( R_s = \sqrt{\frac{\omega \mu_0}{2\pi}} \) is the surface conductor impedance, \( R_p \) is the per-unit length ohmic resistance due to the proximity effect and \( R_0 = \frac{NR_s}{2\pi a} \) is the per-unit length ohmic resistance due to the skin effect. So, the complete relation for computing the radiation efficiency is:

\[
\eta = \frac{R(N^2)}{R(N^2) + R(N)} (1 - |\Gamma|^2)
\]

The following MATLAB script aims to identify the highest possible efficiency within the CubeSat constraints (1 cm as a maximum thickness for the antenna).

```matlab
% Design of a stand-alone, electrically-small, %
% N-turns loop antenna made of Copper and having %
% maximum efficiency within the CubeSat constraints %
% (circular loop with circular cross section) %

clear all
close all
cle

N=4; % number of turns
loopRadius=linspace(0.5,1.1,1000); % loop radius [cm]
```
conductorRadius = linspace(0.1, 1.1, 1000); % conductor radius [mm]

freq = 437; % frequency [MHz]

zeta = 377; % free space impedance [Ohm]

c = 3 * 1e8; % speed of light [m/s]

rho = 1.7e-8; % metal resistivity (copper)

mu0 = 4 * pi * 1e-7;

f = freq * 1e6;
pul = 2 * pi * f;
lambda = c / f;

beta = 2 * pi / lambda;

b = loopRadius / 100;
a = conductorRadius / 1000;
area = pi * b^2;

Rr = zeta * beta^4 / 6 / pi * (N * area) ^ 2;

Rs = sqrt(pul * mu0 / 2 * rho); Ro = N * Rs / (2 * pi * a);

Rp = 0;

Ri = N * b / a * Rs * (Rp / Ro + 1);

maxEff = max(Rr / (Rr + Ri)) * 100
As a conclusion, an electrically small loop antenna working at 437 MHz and coherent with the CubeSat constraints can just provide a 60% efficiency as a maximum result. In the following, electrically large loops are going to be analyzed in order to increase the overall performance.

8.5.3 **Electrically large loop**

When \( \frac{R}{\lambda} > 0.1 \), the radiating system is generally considered as an electrically large loop. This antenna is commonly used when the ratio is approximately unitary (resonant size) and the main application concerns directional arrays. Since the mechanical constraints do not allow such a condition, a matching network will be necessarily developed.
As the dimensions of the loop increase, the current variations along the perimeter must be taken into account and a good distribution is represented by the Fourier series:

\[ I(\phi) = I_{DC} + 2 \sum_{n=1}^{M} I_{n} \cos(n\phi) \]

where \( \phi \) is measured from the feed point of the loop.

The following two graphs (Figure 157 and Figure 158) show the input impedance associated to a circular loop as a function of \( \frac{p}{\lambda} = \frac{2\pi b}{\lambda} = \beta b \) and \( \Omega = 2\ln\left(\frac{2\pi b}{\lambda}\right) \).
Figure 158: Input reactance of a circular loop antenna[9]

It is clear that the first antiresonance occurs when the circumference of the loop is approximately $\frac{\lambda}{2}$ and that is an extremely sharp region. Moreover, as the thickness associated to the wire increases, the reactance changes a lot.
Figure 159: Directivity of an electrically large circular loop antenna when the elevation angle is zero[9]

Figure 159 shows that, as the circumference approaches to one wavelength, the maximum directivity shifts from the loop-plane ($\theta = 90^\circ$) to its axis ($\theta = 0^\circ, 180^\circ$). However, the maximum directivity is approximately 4.5 dB and it occurs when the circumference is about $1.4\lambda$.

In order to achieve a larger antenna compatibility, the constraints concerning the dimensions are set according to the CubeSat standard. As a result, the upper bound for the physical shape is the square having a 9 cm side. The first antiresonant point implies a circular radius equal to 5.46 cm, but that is beyond the CubeSat limit. In order to make the design as resonant as possible and meet the space requirements, a set of parameters is pointed out in Table XLIII.
TABLE XLIII: ELECTRICALLY LARGE CIRCULAR LOOP-ANTENNA OVER PCB

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$b$</td>
<td>4.5 cm</td>
</tr>
<tr>
<td>$a$</td>
<td>45 $\mu$m</td>
</tr>
<tr>
<td>$\Omega$</td>
<td>17.5</td>
</tr>
<tr>
<td>$\beta b$</td>
<td>0.41</td>
</tr>
<tr>
<td>$D_{\theta=0}$</td>
<td>$-0.9dB$</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>$\sim (250 + j3500) \ \Omega$</td>
</tr>
</tbody>
</table>

A final remark refers to the ohmic losses because they have not been taken into account in the theoretical results previously exposed. Regarding this, both electromagnetic computations and measurements generally show significant discrepancies. That is especially around resonance because curves are sharp, then little variations can lead to huge changes.

8.5.4 Simulation

At this point, the goal consists in simulating the last two large circular loops in order to achieve more accurate parameters and compute the efficiency. After that, different geometries are going to be considered to pursue better performance within the AraMiS constraints. ANSYS HFSS software is an industry-standard tool and it is taken as a reference for the following EM simulations.
The set of materials which are considered is reported in Table XLIV.

The first simulation refers to the circular loop antenna which has been theoretically designed in the previous section. In order to develop a suitable structure, an ideally circular loop made of copper is cut and an EM source is placed between the two ends.

After that, a sphere made of air is placed in such a way its external surface is at least \( \frac{\lambda}{2} \) far from the metal structure. Then, the far-field analysis and the modal solution data report are set.
Figure 160: Electromagnetic source in the loop structure (HFSS simulator)

Figure 161: Circular loop orientation (HFSS simulator)
TABLE XLV: ANTENNA SIMULATION 1 - AIR SURROUNDED, PCB-SIZED AND COPPER MADE CIRCULAR LOOP WITH CIRCULAR CROSS SECTION

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( b )</td>
<td>4.5 cm</td>
</tr>
<tr>
<td>( a )</td>
<td>45 ( \mu )m</td>
</tr>
<tr>
<td>( Z_{\text{in}} )</td>
<td>((326 + j4253) \ \Omega)</td>
</tr>
<tr>
<td>( \eta )</td>
<td>59.5%</td>
</tr>
<tr>
<td>( D_{\text{max}} )</td>
<td>1.96 dB</td>
</tr>
</tbody>
</table>

Figure 162: Simulation 1 - circle loop 3D radiation pattern (HFSS simulator)
Figure 163: Simulation 1 - circle loop radiation pattern as a function of the elevation angle (HFSS simulator)

Figure 164: Simulation 1 - circle loop radiation pattern as a function of the longitudinal angle (HFSS simulator)
The great advantage associated to such an antenna is that it can be physically built by means of a microstrip likewise any other trace on the PCB, but the drawback is that the radiation efficiency is not very high. In fact, the $\eta$ is about 60% even if any dielectric substrate has been supposed.

The best benefit in terms of radiation efficiency is achieved by varying the dimensions of the circular structure and the set of parameters is reported in Table XLVI.

**TABLE XLVI: ANTENNA SIMULATION 2 - AIR SURROUNDED AND STAND-ALONE COPPER MADE CIRCULAR LOOP WITH CIRCULAR CROSS SECTION**

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$b$</td>
<td>4.15 cm</td>
</tr>
<tr>
<td>$a$</td>
<td>1.76 mm</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>(1795 + 7308)$ \Omega$</td>
</tr>
<tr>
<td>$\eta$</td>
<td>98%</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>1.94 dB</td>
</tr>
</tbody>
</table>
Figure 165: Simulation 2 - circle loop 3D radiation pattern (HFSS simulator)

Figure 166: Simulation 2 - circle loop radiation pattern as a function of the elevation angle (HFSS simulator)
The drawback associated to this circular loop antenna is the more difficult impedance matching and the need of stand-alone metal structure instead of using a simple PCB trace.

At this point, it is possible to use the electromagnetic simulator in order to analyze different shapes, such as the square one. In this context, $2b$ is the side of the square and $2a$ corresponds to thickness of the metal conductor (results in Table XLVII).
Figure 168: Square loop orientation (HFSS simulator)

### Table XLVII: Antenna Simulation 3 - Air Surrounded and PCB-Sized Copper Made Square Loop with Square Cross Section

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$b$</td>
<td>4.5 cm</td>
</tr>
<tr>
<td>$a$</td>
<td>45 µm</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>$(741 - j4273) \ \Omega$</td>
</tr>
<tr>
<td>$\eta$</td>
<td>80.4%</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>1.79 dB</td>
</tr>
</tbody>
</table>
Figure 169: Simulation 3 - square loop 3D radiation pattern (HFSS simulator)

Figure 170: Simulation 3 - circle loop radiation pattern as a function of the elevation angle (HFSS simulator)
Figure 171: Simulation 3 - circle loop radiation pattern as a function of the longitudinal angle (HFSS simulator)

If the same structure is placed over a 1.3 mm dielectric substrate made of FR-4, the input impedance becomes $Z_{in} = (92 - 1093) \ \Omega$, the peak directivity results $D_{max} = 1.88 \ \text{dB}$ and a lower radiation efficiency appears due to the FR-4 tangent loss ($\eta = 69.5\%$). Since the PCB trace must be necessarily placed over a dielectric substrate, the latter worst case structure is the one to be considered.

The following simulation refers to a square loop antenna whose resistivity approximately equals 50 $\Omega$ in order to make easier the impedance matching.
TABLE XLVIII: ANTENNA SIMULATION 4 - AIR SURROUNDED AND STAND-ALONE COPPER MADE SQUARE LOOP WITH SQUARE CROSS SECTION

<table>
<thead>
<tr>
<th>Simulation 4 - Square</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>Value</td>
</tr>
<tr>
<td>b</td>
<td>4.15 cm</td>
</tr>
<tr>
<td>a</td>
<td>1.76 mm</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>(49 − j930) Ω</td>
</tr>
<tr>
<td>$\eta$</td>
<td>99%</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>1.89 dB</td>
</tr>
</tbody>
</table>

Figure 172: Simulation 4 - square loop 3D radiation pattern (HFSS simulator)
Figure 173: Simulation 4 - circle loop radiation pattern as a function of the elevation angle (HFSS simulator)

Figure 174: Simulation 4 - circle loop radiation pattern as a function of the longitudinal angle (HFSS simulator)
The latter two structures are the ones to be considered for the antenna design because they are the most efficient. Additionally, they are respectively characterized by an easier PCB implementation (square cross section instead of circular) and a good resistive matching ($R_{in} \approx 50 \, \Omega$). Since the radiation efficiency is much higher in the last case (about 100%), that is going to be the final choice for the design.

### 8.5.5 Impedance matching

Once a suitable radiating source is defined, it is necessary to achieve the impedance matching with the electronic systems. According to the specifications regarding both the transceiver and the power amplifier, $50 \, \Omega$ impedance matching must be pursued. *AWR DESIGN ENVIRONMENT* is a microwave-simulator tool and it has been selected for design/optimization of the matching circuits.

By means of the electromagnetic antenna simulator it is possible to compute the antenna impedance, then an ideal transmission line is added to implement a $50 \, \Omega$ electrical adapter. After that, AWR-optimizer allows to determine both the characteristic impedance ($Z_0$) and the electrical length ($L_e$) which, when associated to the transmission line, fully meet a “good” return loss ($RL \leq 20 \, dB$).

\[
\begin{align*}
    RL &= 10\log|s_{11}|^2 \leq 20dB \rightarrow |s_{11}|dB \leq 10dB \\
    EL &= L_e = \beta L = \frac{2\pi}{\lambda_0} \cdot \frac{\lambda_0}{X} L = \frac{2\pi}{\lambda_0} \cdot \frac{f}{f_0} L
\end{align*}
\]

Finally, a physical microstrip having the same length ($L$) and characteristic impedance is automatically determined. In order to achieve a feasible support, a $150 \, \Omega$ upper bound has been set for $Z_0$, so two series transmission lines are needed to reach the goal.
For example, the structure associated to the third simulation can be represented by the schematic of Figure 175.

Once a set of optimal values for both characteristic impedances ($Z_0$) and electrical lengths ($EL$) is determined, it is possible to design the physical microstrips which match the features of the ideal network.
<table>
<thead>
<tr>
<th>TL</th>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL1</td>
<td>$Z_0$</td>
<td>8 Ω</td>
</tr>
<tr>
<td></td>
<td>$L_e$</td>
<td>98.18°</td>
</tr>
<tr>
<td></td>
<td>$W$</td>
<td>2.559 cm</td>
</tr>
<tr>
<td></td>
<td>$L$</td>
<td>9.003 cm</td>
</tr>
<tr>
<td>TL2</td>
<td>$Z_0$</td>
<td>125 Ω</td>
</tr>
<tr>
<td></td>
<td>$L_e$</td>
<td>81.95°</td>
</tr>
<tr>
<td></td>
<td>$W$</td>
<td>186.9 μm</td>
</tr>
<tr>
<td></td>
<td>$L$</td>
<td>9.188 cm</td>
</tr>
</tbody>
</table>

The graph in Figure 177 proves that the “good-matching” specification is met because both the ideal transmission line and the microstrip show a $s_{11}$ parameter which lower than the threshold.

In contrast, the structure associated to the fourth simulation has an input impedance equal to $Z_{in} = (49.4 - j930)$ Ω, so, in order to achieve the resonance, it is sufficient to add a series inductor:

$$Z_L = j2\pi fL = j930\Omega \rightarrow L = 0.33 \mu H$$
8.5.6 Analysis with the complete architecture

In order to compute the antenna parameters associated to the final satellite configuration, it is necessary to add the AraMiS structure and the dielectric support. In the following example (Figure 179), the square loop antenna previously designed is placed over a substrate made of FR4 and that stands above a simple cube made of aluminum. Such a choice is the best one
Figure 179: Complete architecture with the square loop antenna (HFSS simulator)

from the point of view of the mechanical stability since the continuous supporting layer (i.e. the substrate) reduces vibration issues associated to the antenna.

The HFSS simulation points out that the radiation efficiency dramatically drops down from more than 95% to approximately 11%. That is due to both power dissipation through the substrate and to the presence of a metal surface (i.e. the upper face of the cube). As a matter of fact, the metal face acts as a ground plane and it is too close to the antenna if compared to the wavelength. As a result, the square loop results unusable and a new arrangement must be researched to increase performance. Firstly, the radiating system should be fixed to the
**TABLE I: COMPLETE ANTENNA ARCHITECTURE, COMPOSED OF A CUBIC ARAMIS STRUCTURE, FR-4 DIELECTRIC AND THE SQUARE LOOP ANTENNA OF SIMULATION 4**

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Cubic AraMIS</th>
<th>Dielectric</th>
<th>Square-loop antenna</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>165x165x165 mm$^3$</td>
<td>165x165x10 mm$^3$</td>
<td>83x83x3.52 mm$^3$</td>
</tr>
</tbody>
</table>

Figure 180: Complete architecture with the square loop antenna for different offset values.

cube just by using thin dielectric turrets instead of a large surface (at the expense of vibration issues), then the distance between the antenna and the metal plane (offset) must be increased beyond the initial constraint (1 cm). Table I shows how the radiation efficiency and the input impedance change as a function of the offset length.
As a conclusion, the square-loop antenna becomes a feasible radiating system for a cubic AraMiS structure when the offset is at least 2cm ($\eta > 90\%$), while at 3 cm-offset the parasitic dissipation is completely negligible ($\eta = 99\%$).

The comparison between the stand-alone antenna and the complete configuration with 3 cm offset points out two main variations. Firstly, the maximum directivity is now along $z$-axis, then the input impedance is changed and a new matching network is required.
Figure 181: Complete architecture with 3 cm-offset - square loop 3D radiation pattern (HFSS simulator)

Figure 182: Complete architecture with 3 cm-offset - square loop radiation pattern as a function of the elevation angle (HFSS simulator)
Similarly to the case of the stand-alone antenna, there are two ways to achieve the electrical matching and results are collected in Table LIII.

Alternatively, it is possible to reduce the cross section in order to achieve $R_{in} = 50 \, \Omega$ and that happens when the antenna dimensions are $83\times83\times2.5 \, \text{mm}^3$. In such a way, $X_{in} = -j2710 \, \Omega$, then the electrical matching would just require a series inductor $L = 100 \, \mu\text{H}$.
TABLE LI: NETWORK MATCHING FOR THE COMPLETE ANTENNA ARCHITECTURE, COMPOSED OF A CUBIC ARAMIS STRUCTURE AND THE SQUARE LOOP ANTENNA OF SIMULATION 4 WITH 3CM-OFFSET

<table>
<thead>
<tr>
<th>Typology</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series lumped elements</td>
<td>( L = 0.49 , \mu H )</td>
</tr>
<tr>
<td></td>
<td>( R = 35 , \Omega )</td>
</tr>
</tbody>
</table>

Microstrip \( (h_{FR4} = 1.55\text{mm}, \quad t_{Cu} = 90 \, \mu \text{m}, \quad |s_{11}| < -10.9 \, \text{dB}) \)

<table>
<thead>
<tr>
<th>TL1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( Z_0 = 7.8 , \Omega )</td>
</tr>
<tr>
<td></td>
<td>( L_e = 89.92^\circ )</td>
</tr>
<tr>
<td></td>
<td>( W = 3.081 , \text{cm} )</td>
</tr>
<tr>
<td></td>
<td>( L = 8.235 , \text{cm} )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TL2</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( Z_0 = 130 , \Omega )</td>
</tr>
<tr>
<td></td>
<td>( L_e = 84.49^\circ )</td>
</tr>
<tr>
<td></td>
<td>( W = 188.9 , \mu \text{m} )</td>
</tr>
<tr>
<td></td>
<td>( L = 9.477 , \text{cm} )</td>
</tr>
</tbody>
</table>
8.6 **Dipole-antenna design**

8.6.1 **Theoretical description**

Different radiating systems are also analyzed in order to provide alternative solutions. In this context, dipoles are now considered since they have been already adopted for similar space applications. A dipole antenna is a radiating structure that can be made of a *simple wire*, with a *center-fed driven element*. It consists of two lined metal conductors with a small gap in between, where the radio frequency voltage is applied\[8\][13].

![Figure 184: Dipole antenna and coordinate system\[13\]](image)

Similarly to what has been demonstrated for circular loop antennas, electrically short dipoles \((\frac{L}{\lambda} \ll 1)\) show very low radiating resistance and that leads to both difficult impedance matching
and a low radiation efficiency. As a consequence, longer structures with sinusoidal current distribution are now analyzed, then a suitable antenna is going to be designed.

\[
\begin{align*}
E(P) &= \frac{e^{-jkr}}{4\pi r} e(\theta, \phi) \quad \rightarrow \text{electric field} \\
k_0 &= \omega \sqrt{\mu_0 \epsilon_0} \quad \rightarrow \text{vacuum radiating constant} \\
e(\theta, \phi) &\approx j\omega\mu\hat{\theta}(\theta, \phi)\sin\theta I(\theta) \quad \rightarrow \text{linear polarization} \\
I(\theta) &= \int_{-\frac{L}{2}}^{\frac{L}{2}} I(z) e^{jk\cos(\theta)z} dz \quad \rightarrow \text{current integration} \\
I(\pm z) &= I_0^+ e^{-jkz} + I_0^- e^{jkz} \quad \rightarrow \text{sinusoidal current distribution} \\
I(0) &= I_0^+ + I_0^- = I_{\text{source}} \quad \rightarrow \text{current source}
\end{align*}
\]

Figure 185: Radiation patterns for infinitely thin dipoles[13]
As far as $\frac{L}{\lambda}$ increases up to 1, the maximum directivity also goes up without side lobes, while, beyond such a threshold, electromagnetic emission takes place with multiple beams[8]. According to the AraMiS objective, directivity must be low and lower values for $L$ also allow mechanical optimization for the metal structure. Regarding this, when $\frac{L}{\lambda} \leq 0.5$, the input impedance for a circular cross section dipole is approximately given by the following formula:

$$Z_{in} = R(k\frac{L}{2}) - j \left[120 \left(ln\left(\frac{kL}{2\pi}\right) - 1\right)cot(k\frac{L}{2}) - X(k\frac{L}{2})\right]$$

where, $L$ is the total length of the antenna, $a$ is the cross-section radius, $k\frac{L}{2} = \pi\frac{L}{\lambda}$ is measured in radians and the functions $R(k\frac{L}{2})$ and $X(k\frac{L}{2})$ are tabulated in Table LIII.
TABLE LIII: LOOK-UP TABLE FOR THE DIPOLE INPUT IMPEDANCE COMPUTATION

<table>
<thead>
<tr>
<th>$k\frac{L}{2}$ [rad]</th>
<th>$R(k\frac{L}{2})$ [$\Omega$]</th>
<th>$X(k\frac{L}{2})$ [$\Omega$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>0.1506</td>
<td>1.010</td>
</tr>
<tr>
<td>0.2</td>
<td>0.7980</td>
<td>2.302</td>
</tr>
<tr>
<td>0.3</td>
<td>1.821</td>
<td>3.818</td>
</tr>
<tr>
<td>0.4</td>
<td>3.264</td>
<td>5.584</td>
</tr>
<tr>
<td>0.5</td>
<td>5.171</td>
<td>7.141</td>
</tr>
<tr>
<td>0.6</td>
<td>7.563</td>
<td>8.829</td>
</tr>
<tr>
<td>0.7</td>
<td>10.48</td>
<td>10.68</td>
</tr>
<tr>
<td>0.8</td>
<td>13.99</td>
<td>12.73</td>
</tr>
<tr>
<td>0.9</td>
<td>18.16</td>
<td>15.01</td>
</tr>
<tr>
<td>1.0</td>
<td>23.07</td>
<td>17.59</td>
</tr>
<tr>
<td>1.1</td>
<td>28.83</td>
<td>20.54</td>
</tr>
<tr>
<td>1.2</td>
<td>35.60</td>
<td>23.93</td>
</tr>
<tr>
<td>1.3</td>
<td>43.55</td>
<td>27.88</td>
</tr>
<tr>
<td>1.4</td>
<td>52.92</td>
<td>32.20</td>
</tr>
<tr>
<td>1.5</td>
<td>64.01</td>
<td>38.00</td>
</tr>
<tr>
<td>$\frac{\pi}{2}$</td>
<td>73.12</td>
<td>42.46</td>
</tr>
</tbody>
</table>
The best impedance matching is achieved when \( k \frac{L}{2} = 1.4 \) because the real part is as close as possible to 50 Ω. As a result, \( L = 1.4\frac{\lambda}{\pi} \approx 30.57 \text{ cm} \), \( R(k\frac{L}{2}) = 52.92 \text{ Ω} \) and \( X(k\frac{L}{2}) = 32.2 \text{ Ω} \).

Moreover, in order to work at resonance, the radius \( a \) must be equal to:

\[
a = \frac{L}{2} e^{-\left[\frac{X(1.4)}{120 \cot(1.4)} + 1\right]} = \frac{L}{2} e^{-\left[\frac{X(1.4)}{120 \cot(1.4)} + 1\right]} \approx 1.186 \text{ cm}
\]

Although such a solution provides the best results in terms of impedance matching, it is not feasible due to the AraMiS space constraint. As a matter of fact, the dipole can be longer than the physical boundary corresponding to the tile \( (d_{\text{tile}} = 16.5\sqrt{2} \text{ cm} \approx 23.33 \text{ cm}) \) only if its mechanical structure is flexible. For instance, taking advantage from the behaviour associated to any steel-made torsion spring, the antenna can be rolled up around a central support and automatically elongated after deployment. Regarding this, it is necessary to reduce the antenna thickness down to few tenths of a millimeter and the final choice is reported in Table LIV.

| TABLE LIV: \( \frac{1}{2} \)-DIPOLE ANTENNA DESIGN |
|-----------------|--------|
| Quantity        | Amount |
| \( L \)         | 30.57 cm |
| \( a \)         | 0.7 mm  |
| \( Z_{\text{in}} \) | \( (52 - j59) \text{ Ω} \) |
| \( \frac{L}{\lambda} \) | 0.45    |
| \( D_{\text{max}} \) | 2.1 dB  |
8.6.2 Simulations

Theoretical results have been derived using an ideal metal conductor, while the actual radiating system must be made of steel in order to be both flexible and robust. As a result, in order to ensure 50 Ω input resistance, the physical length must be reduced. The antenna parameters are collected in Table LV.

<table>
<thead>
<tr>
<th>TABLE LV: STAND-ALONE AND STAINLESS STEEL MADE $\frac{\lambda}{2}$-DIPOLE SIMULATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standing alone dipole along $y$-axis</td>
</tr>
<tr>
<td>Quantity</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>$Z_{in}$</td>
</tr>
<tr>
<td>$\eta$</td>
</tr>
<tr>
<td>$D_{max}$</td>
</tr>
<tr>
<td>Metal conductor</td>
</tr>
<tr>
<td>Mohs hardness</td>
</tr>
<tr>
<td>Density</td>
</tr>
<tr>
<td>Conductivity</td>
</tr>
</tbody>
</table>
Figure 187: Standing alone dipole - 3D radiation pattern (HFSS simulator)

Figure 188: Standing alone dipole - radiation pattern as a function of the elevation angle (HFSS simulator)
Figure 189: Standing alone dipole - radiation pattern as a function of the longitudinal angle (HFSS simulator)

Figure 190: Complete dipole architecture with 3 cm-offset (HFSS simulator)
TABLE LVI: COMPLETE ANTENNA ARCHITECTURE, COMPOSED OF THE STAINLESS STEEL MADE $\frac{\lambda}{2}$-DIPOLE PLACED OVER A CUBIC ARAMIS STRUCTURE WITH 3 CM OFFSET

<table>
<thead>
<tr>
<th>Complete architecture</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>Value</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>$(12 - j109) \Omega$</td>
</tr>
<tr>
<td>$\eta$</td>
<td>89.7%</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>2.3 dB</td>
</tr>
<tr>
<td>Offset</td>
<td>3 cm</td>
</tr>
<tr>
<td>Metal conductor</td>
<td>Stainless steel</td>
</tr>
<tr>
<td>Mohs hardness</td>
<td>6.5</td>
</tr>
<tr>
<td>Density</td>
<td>$8055 \frac{Kg}{m^3}$</td>
</tr>
<tr>
<td>Conductivity</td>
<td>$1.1 \cdot 10^6 \frac{S}{m}$</td>
</tr>
</tbody>
</table>

The first simulation points out that the radiation pattern is more uniform with respect to that of the loop antenna. Moreover, both efficiency and directivity are equivalent when the dipole is standing alone. In contrast, the simulation with the complete AraMiS architecture highlights that, even by setting the offset distance between the dipole and the metal cube at 3 cm, the efficiency results lower, while the directivity above the metal plane becomes higher.
As a conclusion, the square loop antenna is preferable because it does not require any torsion spring mechanism, it provides higher efficiency and has a lower directivity.

8.7 Monopole-antenna design

8.7.1 Theoretical description

A monopole antenna is a class of radiating systems which consists of a *straight rod-shaped conductor*. That is often mounted perpendicularly over a conductive surface acting as a *ground plane*. The driving signal coming from the transmitter is applied between the lower end of the monopole and the ground plane, as shown in Figure 191.

![Figure 191: Monopole antenna and coordinate system](image-url)
Both the electrical impedance and the radiation characteristics can be inferred from a dipole having double length. In case of a base-driven monopole, the input impedance is equal to one-half that of the center-driven dipole, while the radiation pattern above the infinite ground plane is identical to the upper half of the radiation pattern associated to the corresponding dipole[13].

As a result, in order to ensure 50 Ω as input resistance, the corresponding dipole must have a 100 Ω input resistance. According to the following diagram (Figure 192), such a requirement leads to \( \frac{l}{\lambda} \approx 0.5 \) and \( \frac{l}{d} = 25 \), where \( l = 2L \) and \( d \) is the diameter of the circular cross section.

![Figure 192: Input resistance for a dipole][8]
TABLE LVII: $\frac{1}{4}$-MONOPOLE ANTENNA DESIGN

<table>
<thead>
<tr>
<th>Monopole antenna</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>Amount</td>
</tr>
<tr>
<td>$L$</td>
<td>17.15 cm</td>
</tr>
<tr>
<td>$a$</td>
<td>0.7 mm</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>$(50 + j60) , \Omega$</td>
</tr>
<tr>
<td>$\frac{L}{\lambda}$</td>
<td>0.25</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>2.3 dB</td>
</tr>
</tbody>
</table>

Figure 193: Input reactance for a dipole[8]
In reality, the infinite ground plane is not feasible and, in the AraMiS context, it is replaced by the upper side of the telecommunication tile. In general, the effect of any finite-size ground plane affects both the impedance and the radiation pattern. Such a phenomenon has been analytically studied only over circular metal planes, while the effects due to the square AraMiS tile are just going to be simulated. The impedance variation with respect to the monopole over an infinite ground plane is given by the following equation:

$$\Delta Z = Z - Z_0 = j\frac{60}{kd} e^{-jkd} |k \int_0^h I(z) \frac{I(0)}{I(0)} dz|^2$$

where, $d$ is the diameter of the circular ground plane, $Z_0$ is the impedance in presence of an infinite ground plane, $k = \frac{2\pi}{\lambda}$, $h$ is the height of monopole, $I(z)$ is the current distribution function and $I(0)$ is the input current. When the ground plane has a diameter greater than 10 wavelengths, the variation of the impedance is less than 1 Ω, so $\Delta Z$ becomes negligible.

Since the tile diameter is short when compared to the wavelength, relevant impedance variations are expected in the simulation. Moreover, concerning the physical antenna implementation, the monopole structure must be telescopic in order not to act as a protrusion before the deployment takes place. That leads to a cross section which is not constant and, as a consequence, significant electrical variations could arise.
Figure 194: Universal curve for the impedance variation as a function of the ground plane diameter\cite{8}

8.7.2 Simulations

In order to approximate the “infinite” ground plane, a $9\lambda$-diameter circular surface is used in the following simulation.
TABLE LVIII: \( \frac{1}{4} \)-MONOPOLE ANTENNA SIMULATION WITH AN ELECTRICALLY LARGE GROUND PLANE (9\( \lambda \))

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_{in} )</td>
<td>((47.1 + j54.2) \quad \Omega)</td>
</tr>
<tr>
<td>( \eta )</td>
<td>99.1%</td>
</tr>
<tr>
<td>( D_{max} )</td>
<td>3.8 dB</td>
</tr>
<tr>
<td>Metal conductor</td>
<td>Aluminum</td>
</tr>
<tr>
<td>Orientation</td>
<td>z-axis</td>
</tr>
</tbody>
</table>

Figure 195: Large ground plane - Monopole 3D radiation pattern (HFSS simulator)
Figure 196: Large ground plane - Monopole radiation pattern as a function of the elevation angle (HFSS simulator)

Figure 197: Large ground plane - Monopole radiation pattern as a function of the longitudinal angle (HFSS simulator)
The radiation pattern shows non-negligible power radiation even below the ground plane because that is not infinite. However, the input impedance is coherent with theoretical calculation, so it is now reasonable to analyze how the original antenna behaves over the complete AraMiS architecture.

Figure 198: Complete architecture with monopole antenna (HFSS simulator)
TABLE LIX: COMPLETE ANTENNA ARCHITECTURE, COMPOSED OF THE $\frac{\lambda}{4}$ MONOPOLE ANTENNA AND A CUBIC ARAMIS STRUCTURE

<table>
<thead>
<tr>
<th>Complete architecture</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>Value</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>$(44 - j6) \ \Omega$</td>
</tr>
<tr>
<td>$\eta$</td>
<td>99.4%</td>
</tr>
<tr>
<td>$D_{max}$</td>
<td>1.9 dB</td>
</tr>
<tr>
<td>Metal conductor</td>
<td>Aluminum</td>
</tr>
<tr>
<td>Orientation</td>
<td>$z$-axis</td>
</tr>
</tbody>
</table>

Figure 199: Complete architecture - Monopole 3D radiation pattern (HFSS simulator)
Figure 200: Complete architecture - Monopole radiation pattern as a function of the elevation angle (HFSS simulator)

Figure 201: Complete architecture - Monopole radiation pattern as a function of the longitudinal angle
The latter simulation highlights that the input resistance is not changed very much, while the reactance is now very small. As a result, adopting such an antenna would be beneficial from the electrical-matching point of view. Moreover, beyond the consideration that both efficiency and maximum directivity meet the AraMiS specifications, radiation pattern is omnidirectional over $xy$-plane and that is the greatest advantage with respect to the other previously studied radiating systems. Anyway, since telescopic antennas require additional mechanical efforts due to space constraints and reliability issues, the solution which is going to be chosen is the square loop-antenna.
CHAPTER 9

TESTING

One of the initial goals related to the thesis was to physically implement the UHF telecommunication system. Unfortunately, no construction was carried out for lack of time. However, this chapter is devoted to describe the testing procedure of the electronic board. Firstly, a suitable configuration is proposed in order to achieve measurement points for electrical features and radio frequency TX/RX verification. Secondly, a suitable space qualification test is described according to the CubeSat standard and the facilities which are available at Polytechnic of Turin. Finally, an orbit simulation is carried out in order to retrieve a possible scenario for the radio communication system which has been designed in this thesis.

9.1 Functional tests on the electronic board

The board must be tested in order to check that both the electrical parameters and the communication protocol properly work according to the AraMiS specifications. The set of required instruments and equipment which are going to be used is pointed out in the following list (Figure 202).

- Power supply;
- DSO;
- Multimeter;
- Spectrum analyzer;
• Radio;
• TNC;
• PC.

The first test consists in verifying the correct power distribution to all the integrated circuits. The power supply generator must be connected to the electronic board through the J6-interface (PIN8, PIN9) and a high-level logic signal ($2 - 3$ V) must be applied at PIN16 to enable the load switch. According to the AraMiS specifications regarding the power distribution bus, the voltage at the output of each regulator must be checked (using the multimeter) for different voltage supply points, ranging from 12 V to 18 V. Once the comparison returns coherent values, it is possible to load the housekeeping routines into the microcontroller (through the JTAG interface). Then, it is possible to achieve the corresponding ADC outputs (Table LX) by retrieving the acquisition commands.
After that, a low-level signal applied at PIN16 (J6-interface) must open the load switch, causing the power-off of the entire board ($V_{\text{measured}} = 0 \text{ V}$).

The second test is devoted to check the anti latch-up circuit and that is performed by feeding the electronic board ($V_{\text{supply}} = [12, 18] \text{ V}$) and simulating the SEU with a short circuit to ground. The digital storage oscilloscope must be connected through the probes at the SW- pin of the 1B127 hybrid circuit. After that, the transient analysis must be set in the DSO options. Then SW- can be grounded. The voltage measured by the DSO should drop to zero within $100 \mu\text{s}$, then it should reach again the supply voltage within $10 \text{ ms}$ (recovery time) when the short circuit is removed.

At this point, the following test concerns the radio frequency features in transmitting mode. In particular, the goal is to measure the output power, the central TX frequency and the channel bandwidth. In order to perform those measurements, the SMA90 antenna connector must be connected to the input of the spectrum analyzer, then the microcontroller must be programmed through the JTAG interface. A C++ program is used to set the transceiver in transmitting

### TABLE LX: TEST POINTS FOR POWER MANAGEMENT VERIFICATION

<table>
<thead>
<tr>
<th>Output voltage</th>
<th>$V_{\text{required}} [\text{V}]$</th>
<th>$V_{\text{measured}} [\text{V}]$</th>
<th>$V_{\text{acquired}} [\text{V}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1B131C_Voltage_1</td>
<td>$\sim V_{\text{supply}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reg_3V31</td>
<td>3.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reg_3V01</td>
<td>3.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reg_2V81</td>
<td>2.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PowerDC-DCconv1</td>
<td>3.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
mode, then a long sequence of bits is transmitted. The corresponding modulated carrier should be visualized through the spectrum analyzer.

<table>
<thead>
<tr>
<th>TABLE LXI: TEST POINTS FOR FREQUENCY MANAGEMENT VERIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{supply} = [12, 18], \text{V}$</td>
</tr>
<tr>
<td>Quantity</td>
</tr>
<tr>
<td>-------------------</td>
</tr>
<tr>
<td>Output Power</td>
</tr>
<tr>
<td>Central frequency</td>
</tr>
<tr>
<td>Bandwidth</td>
</tr>
</tbody>
</table>

Finally, it is necessary to test the communication protocol through an actual point-to-point data exchange. Regarding this, the SMA90 antenna connector must be connected to the input of the radio (tuned at 437 MHz) and the radio must be connected to the TNC. The latter device manages the AX.25 protocol, computes the FCS and modulates/demodulates the 9.6 Kbps data stream coming from/going to the PC (i.e. the ground station). At this point, the entire control software can be loaded into the electronic board through the JTAG interface and it is possible to build up a data exchange with the PC. If received packets and transmitted ones coincide, the data-link properly works.
9.2 Space environment and launch qualification

Beyond functional tests, tiles are fully qualified by means of in-house testing equipment. Qualification is crucial to assure that systems can work in the space environment and they are not damaged during the launch.

Nowadays, the only small-satellite standard on the market is CubeSat and the corresponding test model basically takes into account the following procedure:

- *random vibration* of 14.1G along the three axis for 10 minutes;
- *thermal test* ranging from −20 °C to 70 °C;
- *outgassing* in high vacuum (< 0.013 Pa), from room temperature to a maximum temperature equal to 70 °C for 2 hours.

Similarly, a set of testing facilities is present at Polytechnic of Turin in order to perform space environment and launch qualification for the AraMiS architecture.

Firstly, there is a vibration equipment setup which is handled by a PC and it is based on a permanent magnet vibration system (Figure 203).

The shaker (*LDS V455/6*) is driven by a suitable signal amplifier (*PA 1000L*) and vibrations propagate to the tile under test through the vibrating table. A vibration control loop is built up by means of accelerometers which monitor the state of the tile and send data to the control box (*LDS LASER USB*).
TABLE LXII: VIBRATION FACILITY LIMITS FOR VIBRATION TEST

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force peak</td>
<td>489 N</td>
</tr>
<tr>
<td>Frequency bandwidth</td>
<td>3 KHz</td>
</tr>
<tr>
<td>Maximum acceleration (1 Kg tile mass)</td>
<td>12G</td>
</tr>
<tr>
<td>Displacement (1 Kg tile mass)</td>
<td>14 mm</td>
</tr>
<tr>
<td>Simultaneous tests on the axis</td>
<td>z - single axis</td>
</tr>
</tbody>
</table>

Figure 204 points out the limit acceleration provided by the shaker as a function of frequency. In order to have a comparison, it is remarkable that the ESA standard envelope is 10 times higher in magnitude up to 60 Hz, while it is 10 times lower at frequency ranging from 60 Hz to 3 KHz[4].

Secondly, at Polytechnic of Turin it is possible to perform fast thermal tests using a thermal chamber. In this location the temperature ramp, that is the per minute temperature variation, is uncontrolled but very sharp (thermal shocks). In contrast, more gradual and accurate thermal-
vacuum tests can be carried out using the vacuum pump in the climatic chamber. As a matter of fact, such a facility allows to test pre-defined temperature profiles.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum level for temperature profiles</td>
<td>300 Pa</td>
</tr>
<tr>
<td>Temperature range</td>
<td>−40, 140°C</td>
</tr>
<tr>
<td>Temperature ramp</td>
<td>±3°C/ min</td>
</tr>
</tbody>
</table>

Outgassing in vacuum, that is the release of a gas that was previously dissolved, trapped, frozen or absorbed in some materials (e.g. oxygen in the metal structures made of aluminum),
cannot be tested using such an apparatus because the partial vacuum pressure (300 Pa) is still too high.

9.3 Orbit simulation

As a conclusion of this thesis, AGI STK space-simulation tool is used to achieve some results in terms of both real-time satellite positioning and communication link.

The starting point consists in determining the set of orbital parameters associated to the spacecraft and, regarding this, it is important to remind that the final orbit is not known a priori. As a matter of fact, AraMiS will never be the main payload of the launcher due to low-cost issues, so the deployment coordinates need to be determined afterward. Within a few days after the deployment procedure, the American NORAD system identifies all the orbital parameters associated to the satellite and they are shared on the NORAD website. Once those
data are received by the mission controller, it is possible to simulate its position as a function of time by means of AGI STK.

In the following description (Table LXIV), a random set of orbital parameters is assumed and two GENSO ground stations (one in Turin-Italy and the second one in Chicago-U.S.A.) are supposed to communicate with the AraMiS-UHF channel designed in this thesis. The two ground stations are supposed to have tracking capability and the specifications of the previously described Polytechnic-base-station.

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inclination</td>
<td>70°</td>
</tr>
<tr>
<td>Altitude</td>
<td>600 Km</td>
</tr>
<tr>
<td>RAAN</td>
<td>0°</td>
</tr>
<tr>
<td>Shape</td>
<td>Circular</td>
</tr>
<tr>
<td>Start Time</td>
<td>April 1st, 2012</td>
</tr>
</tbody>
</table>

Figure 207 shows that, by setting a 10° minimum elevation angle for both the ground stations, the coverage areas include the great majority of European countries and both central and eastern regions of the United States. Moreover, as far as the inclination angle goes down (lower than 90°), the coverage area decreases since it results compressed around the equatorial line. As a result, polar orbits are the most preferred ones because they allow a total Earth’s surface coverage.
Figure 206: AraMiS scenario (STK environment)

Figure 207: Ground stations coverage (STK environment)
By keeping as a reference a 5-days long timeframe, the coverage intervals for such a configuration are shown in Figure 208.

The mean duration of the active line of sight is approximately equal to 406 s, while the minimum duration is about 77 s long. As a consequence, the transmission protocol must comply such a constraint by considering different levels of message priority in the communication link.

If the on-board computer shares the future coverage intervals with the mission controller, it is possible to optimize pure elaboration times (e.g. data compression and maneuvers for attitude...
control) when the satellite is not visible by any ground station. In contrast, small housekeeping messages can be sent even in the shortest active intervals. The total active duration within the considered timeframe is 236', so approximately 16.2 MB are available for both header and information fields. Obviously, increasing the number of GENSO base stations would allow to continuously track the satellite with a consequent increasing of the system throughput.
CHAPTER 10

CONCLUSIONS

This thesis was devoted to the complete development of a bidirectional telecommunication system for space applications. The module was supposed to be integrated within the AraMiS architecture, that is an innovative philosophy of small satellites based on tile-modularity and the use of low-cost commercial components.

The objective was to design the electronic board, the antenna apparatus and the software architecture in order to handle both the communication protocol and the housekeeping functions.

The hardware design has been carried out according to the top-down approach and all the theoretical computations have been performed with MATLAB. Technical choices related to frequency selection, modulations and suitable equipment have been taken and justified according to the power budget, the project constraints (i.e. AraMiS mechanical structure and the space related issues) and the availability of specific products on market. Then, a set of devices has been analyzed in terms of the corresponding key-parameters in order to filter the most appropriate ones for each goal.

By means of specific CAD tools (Mentor Graphics and Texas Instruments reference applications), both schematics and the PCB design have been performed. In this context, the PCB stack-up has been selected according to the radio frequency requirements and the Eurocircuit manufacturer’s standard for minimizing costs. Moreover, in order to ensure impedance matching in the microwave range, suitable circuits have been properly designed with AWR.
After that, the C++ control software has been designed in order to drive the communication system, the processing unit and all the housekeeping sensors. Since only COTS components have been used due to the low-cost objective and these are neither space dedicated nor radiation robust, both protection circuits and specific software routines have been implemented in order to ensure a fail operational system. Such a precaution is fundamental to prevent the mission failure in case of SEUs.

The communication protocol selected for this application has been Packet Radio because it is the current standard in packet-based radio amateur digital communication. Regarding this, specific software routines have been implemented to manage the packet assembly/disassembly, then a deep study related to the CRC computation has been carried out. Both the hardware and the software CRC implementations are proposed, but the SW byte-wise algorithm has been finally chosen since the RISC microcontroller is optimized to work within such a framework.

After that, the propagation environment has been studied and the most common UHF radiating systems for satellite-ground communication have been briefly described. Finally, a suitable AraMiS antenna has been designed to ensure both impedance matching and high radiation efficiency in the band of interest. Regarding this, several configurations (i.e. circle/square loops, monopoles and dipoles) have been studied with the HFSS electromagnetic simulator. All the radiating systems have been considered both standing alone and within the AraMiS architecture in the basic cubic shape.

In order to assure the system compatibility within the AraMiS framework and a full technical integration with the other subsystems, a UML description for the entire project documentation
has been developed and steadily updated in the project library. In this thesis, Visual Paradigm has been the reference software for the UML description and the automatic code generation.

In the last sections of the thesis, a brief description of the testing procedure has been highlighted and a high level TX/RX simulation has been shown. The latter has been carried out with the STK space simulator and it assumes the satellite is correctly deployed in a LEO orbit (600 Km of altitude).

As a conclusion, the complete software architecture, all the schematics and the gerber files for the PCB implementation have been provided. In order to resume the parts selection, all the required electronic ICs and hybrids which fully meet the project specifications are now listed:

- TI-CC1020 transceiver;
- TI-MSP430F5438 microcontroller;
- RF6886 power amplifier;
- SKY-13290-313LF antenna switch;
- FOX924B oscillator;
- TI-TPS5450 step down converter;
- TI-LM317 linear regulator;
- 1B127 anti latch-up circuit.

Regarding the on-board radiating system design, the final choice is a copper made square-loop antenna having the following dimensions: 83x83x2.5 mm$^3$. As a matter of fact, the 50
Ω impedance matching is simply achieved by means of a 100 µH series inductor, while good radiation features have been pointed out by the corresponding HFSS simulation:

- $\eta > 90\%$
- $D_{\text{max}} = 1.9 \text{ dB}$

Although the project design has been fully carried out, the physical implementation is currently missing for lack of time. As a consequence, the future work is now supposed to be the final system implementation, in order to test the electrical parameters, the expected functions and the space qualification with the testing facilities at Polytechnic of Turin.
Appendix A

CC1020 PACKAGE AND PINS DESCRIPTION
Figure 209: CC1020 package [15]
### Appendix A (continued)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Pin type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>AGND</td>
<td>Ground (analog)</td>
<td>Exposed die attached pad. Must be soldered to a solid ground plane as this is the ground connection for all analog modules. See page 64 for more details.</td>
</tr>
<tr>
<td>1</td>
<td>PCLK</td>
<td>Digital input</td>
<td>Programming clock for SPI configuration interface</td>
</tr>
<tr>
<td>2</td>
<td>DOI</td>
<td>Digital input</td>
<td>Programming data input for SPI configuration interface</td>
</tr>
<tr>
<td>3</td>
<td>PDO</td>
<td>Digital output</td>
<td>Programming data output for SPI configuration interface</td>
</tr>
<tr>
<td>4</td>
<td>DGND</td>
<td>Ground (digital)</td>
<td>Ground connection (0 V) for digital modules and digital I/O</td>
</tr>
<tr>
<td>5</td>
<td>DVDD</td>
<td>Power (digital)</td>
<td>Power supply (3 V typical) for digital modules and digital I/O</td>
</tr>
<tr>
<td>6</td>
<td>DGND</td>
<td>Ground (digital)</td>
<td>Ground connection (0 V) for digital modules (substrate)</td>
</tr>
<tr>
<td>7</td>
<td>DCLK</td>
<td>Digital output</td>
<td>Clock for data in both receive and transmit mode. Can be used as receive data output in asynchronous mode.</td>
</tr>
<tr>
<td>8</td>
<td>DIO</td>
<td>Digital input/output</td>
<td>Data input in transmit mode; data output in receive mode. Can also be used to start power-up sequencing in receive</td>
</tr>
<tr>
<td>9</td>
<td>LOCK</td>
<td>Digital output</td>
<td>PLL Lock indicator, active low. Output is asserted (low) when PLL is in lock. The pin can also be used as a general digital output, or as receive data output in synchronous NRZ/Manchester mode</td>
</tr>
<tr>
<td>10</td>
<td>XOSC_Q1</td>
<td>Analog input</td>
<td>Crystal oscillator or external clock input</td>
</tr>
<tr>
<td>11</td>
<td>XOSC_Q2</td>
<td>Analog output</td>
<td>Crystal oscillator</td>
</tr>
<tr>
<td>12</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for crystal oscillator</td>
</tr>
<tr>
<td>13</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for the IF VGA</td>
</tr>
<tr>
<td>14</td>
<td>LNA_EN</td>
<td>Digital output</td>
<td>General digital output. Can be used for controlling an external LNA if higher sensitivity is needed.</td>
</tr>
<tr>
<td>15</td>
<td>PA_EN</td>
<td>Digital output</td>
<td>General digital output. Can be used for controlling an external PA if higher output power is needed.</td>
</tr>
<tr>
<td>16</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for global bias generator and IF anti-alias filter</td>
</tr>
<tr>
<td>17</td>
<td>R_BIAS</td>
<td>Analog output</td>
<td>Connection for external precision bias resistor (82 kΩ ± 1%)</td>
</tr>
<tr>
<td>18</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for LNA input stage</td>
</tr>
<tr>
<td>19</td>
<td>RF_IN</td>
<td>RF input</td>
<td>RF signal input from antenna (external AC-coupling)</td>
</tr>
<tr>
<td>20</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for LNA</td>
</tr>
<tr>
<td>21</td>
<td>RF_OUT</td>
<td>RF output</td>
<td>RF signal output to antenna</td>
</tr>
<tr>
<td>22</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for LO buffers, mixers, prescaler, and first PA stage</td>
</tr>
<tr>
<td>23</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for VCO</td>
</tr>
<tr>
<td>24</td>
<td>VC</td>
<td>Analog input</td>
<td>VCO control voltage input from external loop filter</td>
</tr>
<tr>
<td>25</td>
<td>AGND</td>
<td>Ground (analog)</td>
<td>Ground connection (0 V) for analog modules (guard)</td>
</tr>
<tr>
<td>26</td>
<td>AD_REF</td>
<td>Power (analog)</td>
<td>3 V reference input for ADC</td>
</tr>
<tr>
<td>27</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for charge pump and phase detector</td>
</tr>
<tr>
<td>28</td>
<td>CHG_OUT</td>
<td>Analog output</td>
<td>PLL charge pump output to external loop filter</td>
</tr>
<tr>
<td>29</td>
<td>AVDD</td>
<td>Power (analog)</td>
<td>Power supply (3 V typical) for ADC</td>
</tr>
<tr>
<td>30</td>
<td>DGND</td>
<td>Ground (digital)</td>
<td>Ground connection (0 V) for digital modules (guard)</td>
</tr>
<tr>
<td>31</td>
<td>DVDD</td>
<td>Power (digital)</td>
<td>Power supply connection (3 V typical) for digital modules</td>
</tr>
<tr>
<td>32</td>
<td>PSEL</td>
<td>Digital input</td>
<td>Programming chip select, active low, for configuration interface. Internal pull-up resistor.</td>
</tr>
</tbody>
</table>

Figure 210: CC1020 pin description[15]
Appendix B

CC1020 APPLICATION CIRCUIT AND EXTERNAL COMPONENTS
The LC filter can be inserted in the TX path in order to reduce the harmonic emission (Figure 211).

An alternative is to insert the LC filter between the antenna and the RF switch as shown in Figure 212. Such a filter will reduce the spurious emissions as well as increase the receiver selectivity. In contrast, the system sensitivity will be slightly reduced due to the insertion loss of the LC filter.
Figure 212: CC1020 passive network with LC filter between RF switch and antenna [15]

<table>
<thead>
<tr>
<th>Ref</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>LNA input match and DC block</td>
</tr>
<tr>
<td>C3</td>
<td>PA output match and DC block</td>
</tr>
<tr>
<td>C4</td>
<td>Crystal load capacitor</td>
</tr>
<tr>
<td>C5</td>
<td>Crystal load capacitor</td>
</tr>
<tr>
<td>C6</td>
<td>PLL loop filter capacitor</td>
</tr>
<tr>
<td>C7</td>
<td>PLL loop filter capacitor (may be omitted for highest loop bandwidth)</td>
</tr>
<tr>
<td>C8</td>
<td>PLL loop filter capacitor (may be omitted for highest loop bandwidth)</td>
</tr>
<tr>
<td>C80</td>
<td>Decoupling capacitor</td>
</tr>
<tr>
<td>L1</td>
<td>LNA match and DC bias (ground)</td>
</tr>
<tr>
<td>L2</td>
<td>PA match and DC bias (supply voltage)</td>
</tr>
<tr>
<td>R1</td>
<td>Precision resistor for current reference generator</td>
</tr>
<tr>
<td>R2</td>
<td>PLL loop filter resistor</td>
</tr>
<tr>
<td>R3</td>
<td>PLL loop filter resistor</td>
</tr>
<tr>
<td>R10</td>
<td>PA output match</td>
</tr>
<tr>
<td>XTAL</td>
<td>Crystal</td>
</tr>
</tbody>
</table>

Figure 213: Description of passive components in the CC1020 structure [15]
Appendix B (continued)

Input/Output matching

L1 and C1 are the input match for the receiver. L1 is also a DC choke for biasing. L2 and C3 are used to match the transmitter to 50 Ω. Internal circuitry makes it possible to connect the input and output together and match the CC1020 to 50 Ω in both RX and TX mode. However, it is recommended to use an external RF switch for optimum performance.

Bias resistor

The precision bias resistor R1 is used to set an accurate bias current.

PLL loop filter

The loop filter consists of two resistors (R2 and R3) and three capacitors (C6-C8). C7 and C8 may be omitted in applications where high loop bandwidth is desired.

Crystal

An external crystal with two loading capacitors (C4 and C5) is used for the crystal oscillator.

Additional filtering

Additional external components (e.g. RF LC or SAW filter) may be used in order to improve the performance in specific applications.

Power supply decoupling and filtering

External components for power supply decoupling and filtering must be used (not shown in the application circuit).
Appendix C

CONFIGURATION REGISTERS AND TIMING DESCRIPTION FOR

CC1020 INTERFACE
Appendix C (continued)

Figure 214: CC1020 - Configuration registers write operation[15]

Figure 215: CC1020 - Configuration registers read operation[15]
### Figure 216: CC1020 interface - Timing description [15]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCLK, clock frequency</td>
<td>F_{PCLK}</td>
<td>10</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCLK low pulse duration</td>
<td>T_{CL/LH}</td>
<td>50</td>
<td>ns</td>
<td></td>
<td>The minimum time PCLK must be low.</td>
</tr>
<tr>
<td>PCLK high pulse duration</td>
<td>T_{CNH}</td>
<td>50</td>
<td>ns</td>
<td></td>
<td>The minimum time PCLK must be high.</td>
</tr>
<tr>
<td>PSEL setup time</td>
<td>T_{SS}</td>
<td>25</td>
<td>ns</td>
<td></td>
<td>The minimum time PSEL must be low before positive edge of PCLK.</td>
</tr>
<tr>
<td>PSEL hold time</td>
<td>T_{PH}</td>
<td>25</td>
<td>ns</td>
<td></td>
<td>The minimum time PSEL must be held low after the negative edge of PCLK.</td>
</tr>
<tr>
<td>PSEL high time</td>
<td>T_{SH}</td>
<td>50</td>
<td>ns</td>
<td></td>
<td>The minimum time PSEL must be high.</td>
</tr>
<tr>
<td>PDI setup time</td>
<td>T_{DD}</td>
<td>25</td>
<td>ns</td>
<td></td>
<td>The minimum time data on PDI must be ready before the positive edge of PCLK.</td>
</tr>
<tr>
<td>PDI hold time</td>
<td>T_{HD}</td>
<td>25</td>
<td>ns</td>
<td></td>
<td>The minimum time data must be held at PDI, after the positive edge of PCLK.</td>
</tr>
<tr>
<td>Rise time</td>
<td>T_{rise}</td>
<td>100</td>
<td>ns</td>
<td></td>
<td>The maximum rise time for PCLK and PSEL</td>
</tr>
<tr>
<td>Fall time</td>
<td>T_{fall}</td>
<td>100</td>
<td>ns</td>
<td></td>
<td>The maximum fall time for PCLK and PSEL</td>
</tr>
</tbody>
</table>

**Note:** The setup and hold times refer to 50% of VDD. The rise and fall times refer to 10% / 90% of VDD. The maximum load that this table is valid for is 20 pF.
Appendix D

MSP430F1121A PACKAGE AND PINS DESCRIPTION
Appendix D (continued)

Figure 217: MSP430F1121A - ADW, PW, or DGV package[17]

Figure 218: MSP430F1121A - RGE package[17]
## Appendix D (continued)

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NAME</th>
<th>NO.</th>
<th>DW, PW, OR DGV</th>
<th>RGE</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.0/TA0</td>
<td>13</td>
<td>8</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.1/TA0</td>
<td>14</td>
<td>9</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.2/TA1</td>
<td>15</td>
<td>10</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.3/TA2</td>
<td>16</td>
<td>11</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.4/SMCLK/TCK</td>
<td>17</td>
<td>12</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.5/T0/TMS</td>
<td>18</td>
<td>13</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.6/TA1/TC0</td>
<td>19</td>
<td>14</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P1.7/TA2/TDO/TDI</td>
<td>20</td>
<td>15</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P2.0/A0</td>
<td>21</td>
<td>16</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P2.1/A1</td>
<td>22</td>
<td>17</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P2.2/CAOUT/TA0</td>
<td>23</td>
<td>18</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P2.3/CA0/TA1</td>
<td>24</td>
<td>19</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P2.4/CA1/TA2</td>
<td>25</td>
<td>20</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>P2.5/AOS</td>
<td>26</td>
<td>21</td>
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<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>RSTN</td>
<td>27</td>
<td>22</td>
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<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>TEST</td>
<td>28</td>
<td>23</td>
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<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>VCC</td>
<td>29</td>
<td>24</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>VSS</td>
<td>30</td>
<td>25</td>
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<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>XIN</td>
<td>31</td>
<td>26</td>
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<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>XOUT</td>
<td>32</td>
<td>27</td>
<td></td>
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<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>GFIN Pad</td>
<td>33</td>
<td>28</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
<tr>
<td>Package Pad</td>
<td>34</td>
<td>29</td>
<td></td>
<td></td>
<td>I/O</td>
<td>General-purpose I/O/T0 input, T0 clock input, TACLK input</td>
</tr>
</tbody>
</table>

Note: TDO or TDI is selected via JTAG instructions.

Figure 219: MSP430F1121A - Pin description[17]
Appendix E

AX.25 FRAME STRUCTURE DETAILS
Appendix E (continued)

In Figure 220, any “y” indicates that all bit combinations are used in the corresponding bit position.

Moreover, Figure 221 and Figure 222 point out the frame composition associated to AX.25. In this context, the following list provides a brief bit description.

- Bit 0 is the first bit to be sent and bit 7 (or bit 15 for modulo 128) is the last bit to be sent in the control field;
- N(S) is the sent sequence number (bit 1 is the LSB);
- N(R) is the last received sequence number [bit 5 (or bit 9 for modulo 128) is the LSB];
- The “S” bits are the supervisory function bits. Supervisory frames have bit 0 in the control field set to 1-logic and bit 1 set to 0-logic. S frames provide supervisory link control such as acknowledging or requesting retransmission of I frames.
- The “M” bits are the unnumbered frame modifier bits. Unnumbered frames have both bits 0 and 1 of the control field set to 1-logic. U frames are responsible for maintaining additional control over the link beyond what is accomplished with S frames and for establishing and terminating link connections.
- The P/F bit is the Poll/Final bit. The P/F bit is used in all types of frames and it is also used in a command (poll) mode to request an immediate reply to a frame. The reply to this poll is indicated by setting the response (final) bit in the appropriate frame. When not used, the P/F bit is set to “0".
### Figure 220: AX.25 - PID definitions

<table>
<thead>
<tr>
<th>HEX</th>
<th>M</th>
<th>L</th>
<th>S</th>
<th>S</th>
<th>E</th>
<th>Translation</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;&quot;</td>
<td>yy01yyyy</td>
<td>AX.25 layer 3 implemented.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;&quot;</td>
<td>yy10yyyy</td>
<td>AX.25 layer 3 implemented.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x01</td>
<td>00000001</td>
<td>ISO 8208/CCITT X.25 PLP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x06</td>
<td>00000110</td>
<td>Compressed TCP/IP packet. Van Jacobson (RFC 1144)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x07</td>
<td>00000111</td>
<td>Uncompressed TCP/IP packet. Van Jacobson (RFC 1144)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x08</td>
<td>00001000</td>
<td>Segmentation fragment</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xC3</td>
<td>11000011</td>
<td>TEXNET datagram protocol</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xC4</td>
<td>11000100</td>
<td>Link Quality Protocol</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xCA</td>
<td>11001010</td>
<td>Appletalk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xCB</td>
<td>11001011</td>
<td>Appletalk ARP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xCC</td>
<td>11001100</td>
<td>ARPA Internet Protocol</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xCD</td>
<td>11001101</td>
<td>ARPA Address resolution</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xCE</td>
<td>11001110</td>
<td>FlexNet</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xCF</td>
<td>11001111</td>
<td>NET/ROM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xF0</td>
<td>11110000</td>
<td>No layer 3 protocol implemented.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xFF</td>
<td>11111111</td>
<td>Escape character. Next octet contains more Level 3 protocol information.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Escape character. Next octet contains more Level 3 protocol information.</td>
<td>00001000</td>
<td>Escape character. Next octet contains more Level 3 protocol information.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Appendix E (continued)

#### Figure 221: AX.25 - Control-field formats (modulo 8)[3]

<table>
<thead>
<tr>
<th>Control Field Type</th>
<th>Control-Field Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>I Frame</td>
<td>N(R) P N(S) 0</td>
</tr>
<tr>
<td>S Frame</td>
<td>N(R) P/F S S 0 1</td>
</tr>
<tr>
<td>U Frame</td>
<td>M M M P/F M M 1 1</td>
</tr>
</tbody>
</table>

#### Figure 222: AX.25 - Control-field formats (modulo 128)[3]

<table>
<thead>
<tr>
<th>Control Field Type</th>
<th>Control-Field Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>15 14 13 12 11 10  9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>I Frame</td>
<td>N(R) P N(S) 0</td>
</tr>
<tr>
<td>S Frame</td>
<td>N(R) P/F 0 0 0 0 S S 0 1</td>
</tr>
</tbody>
</table>
Appendix F

POWER REGULATOR
Figure 223: TPS5450 - Pin description[19]

Figure 224 points out the main units which compose the integrated circuit and the following paragraphs provide a brief description for each of those.

**Oscillator frequency**

The internal free running oscillator sets the PWM switching frequency at 500 KHz. Such a switching frequency is fixed and allows less output inductance for the same output ripple requirements.

**Voltage reference**

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

**Enable (ENA) and Internal Slow Start**

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts and the internal slow start begins to ramp. If...
the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V will disable the regulator and activate the shutdown mode. The quiescent current of the TPS5450 in shutdown mode is typically 18 µA. The ENA pin has an internal pullup current source, allowing the user to float the ENA pin.

**PWM control**

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier. Then, the error voltage is compared to the ramp voltage by
Appendix F (continued)

the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

Overcurrent limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay.

Overvoltage limiting

The TPS5450 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of \(112.5\% \cdot V_{REF}\). Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.
Appendix G

MSP430F5438 PACKAGE AND PINS DESCRIPTION
Appendix G (continued)

Figure 225: MSP430F5438 - Package[18]
Figure 226: MSP430F5438 - Pin description (1/5)[18]
<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2.1/TA1.0</td>
<td>26 26</td>
<td>General-purpose digital I/O with port interrupt TA1 CCR0 capture, CC1SA input, compare, Out1 output</td>
</tr>
<tr>
<td>P2.2/TA1.1</td>
<td>27 27</td>
<td>General-purpose digital I/O with port interrupt TA1 CCR1 capture, CC1TA input, compare, Out1 output</td>
</tr>
<tr>
<td>P2.3/TA1.2</td>
<td>28 28</td>
<td>General-purpose digital I/O with port interrupt TA1 CCR2 capture, CC1E input, compare, Out1 output</td>
</tr>
<tr>
<td>P2.4/RTCCCLK</td>
<td>29 29</td>
<td>General-purpose digital I/O with port interrupt RTCCCLK output</td>
</tr>
<tr>
<td>P2.5</td>
<td>30 32</td>
<td>General-purpose digital I/O with port interrupt</td>
</tr>
<tr>
<td>P2.6/ACLK</td>
<td>31 33</td>
<td>General-purpose digital I/O with port interrupt ACLK output (divided by 1, 2, 4, 5, 10, or 32)</td>
</tr>
<tr>
<td>P2.7/ADC12CLK/DMAEO</td>
<td>32 34</td>
<td>General-purpose digital I/O with port interrupt Conversion clock output ADC, DMA external trigger input</td>
</tr>
<tr>
<td>P3.0/UCB0STE/UCAD0CLK</td>
<td>33 35</td>
<td>General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode</td>
</tr>
<tr>
<td>P3.1/UCB0SIMO/UCB0SDA</td>
<td>34 36</td>
<td>General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode</td>
</tr>
<tr>
<td>P3.2/UCB0SIMI/UCB0SCL</td>
<td>35 37</td>
<td>General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode</td>
</tr>
<tr>
<td>P3.3/UCB0CLK/UCAD0STE</td>
<td>36 38</td>
<td>General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode</td>
</tr>
<tr>
<td>D/VSS3</td>
<td>37 39</td>
<td>Digital ground supply</td>
</tr>
<tr>
<td>D/VCC3</td>
<td>38 31</td>
<td>Digital power supply</td>
</tr>
<tr>
<td>P3.4/UCAD0TXD/UCAD0SIMO</td>
<td>39 39</td>
<td>General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode</td>
</tr>
<tr>
<td>P3.5/UCAD0RXD/UCAD0SIMI</td>
<td>40 40</td>
<td>General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode</td>
</tr>
<tr>
<td>P3.6/UCB1STE/UCAD1CLK</td>
<td>41 41</td>
<td>General-purpose digital I/O Slave transmit enable – USCI_B1 SPI mode Clock signal input – USCI_A1 SPI slave mode Clock signal output – USCI_A1 SPI master mode</td>
</tr>
<tr>
<td>P3.7/UCB1SIMO/UCB1SDA</td>
<td>42 42</td>
<td>General-purpose digital I/O Slave in, master out – USCI_B1 SPI mode I2C data – USCI_B1 I2C mode</td>
</tr>
<tr>
<td>P4.0/TB0.0</td>
<td>43 43</td>
<td>General-purpose digital I/O TB0 capture CCR0, CC1DA/CC1DB input, compare, Out0 output</td>
</tr>
<tr>
<td>P4.1/TB0.1</td>
<td>44 44</td>
<td>General-purpose digital I/O TB0 capture CCR1, CC1DA/CC1HB input, compare, Out1 output</td>
</tr>
<tr>
<td>P4.2/TB0.2</td>
<td>45 45</td>
<td>General-purpose digital I/O TB0 capture CCR2, CC1E input, compare, Out2 output</td>
</tr>
<tr>
<td>P4.3/TB0.3</td>
<td>46 46</td>
<td>General-purpose digital I/O TB0 capture CCR3, CC1F input, compare, Out3 output</td>
</tr>
<tr>
<td>P4.4/TB0.4</td>
<td>47 47</td>
<td>General-purpose digital I/O TB0 capture CCR4, CC1E input, compare, Out4 output</td>
</tr>
<tr>
<td>P4.5/TB0.5</td>
<td>48 48</td>
<td>General-purpose digital I/O TB0 capture CCR5, CC1F input, compare, Out5 output</td>
</tr>
</tbody>
</table>

Figure 227: MSP430F5438 - Pin description (2/5) [18]
<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NO.</th>
<th>I/O(1)</th>
<th>DESCRIPTION</th>
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</thead>
<tbody>
<tr>
<td>P4.6/TB6.6</td>
<td>49</td>
<td>52</td>
<td>I/O</td>
</tr>
<tr>
<td>P4.7/TB6CLK/SMCLK</td>
<td>50</td>
<td>53</td>
<td>I/O</td>
</tr>
<tr>
<td>P5.4/UCB1SOMI/UCB1SCL</td>
<td>51</td>
<td>54</td>
<td>I/O</td>
</tr>
<tr>
<td>P5.5/UCB1CLK/UCB1SSTE</td>
<td>52</td>
<td>55</td>
<td>I/O</td>
</tr>
<tr>
<td>P5.6/UCB1TXD/UCB1SIMO</td>
<td>53</td>
<td>56</td>
<td>I/O</td>
</tr>
<tr>
<td>P5.7/UCB1RXD/UCB1SOMI</td>
<td>54</td>
<td>57</td>
<td>I/O</td>
</tr>
<tr>
<td>P7.2/TB9OUT/SVMOUT</td>
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<td>59</td>
<td>I/O</td>
</tr>
<tr>
<td>P7.3/TA1.2</td>
<td>56</td>
<td>59</td>
<td>I/O</td>
</tr>
<tr>
<td>P8.0/TA0.0</td>
<td>57</td>
<td>60</td>
<td>I/O</td>
</tr>
<tr>
<td>P8.1/TA0.1</td>
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<td>61</td>
<td>I/O</td>
</tr>
<tr>
<td>P8.2/TA0.2</td>
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<td>62</td>
<td>I/O</td>
</tr>
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<td>P8.3/TA0.3</td>
<td>60</td>
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<td>I/O</td>
</tr>
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<td>P8.4/TA0.4</td>
<td>61</td>
<td>64</td>
<td>I/O</td>
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<tr>
<td>VCORE(2)</td>
<td>62</td>
<td>49</td>
<td>I/O</td>
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<tr>
<td>DVSS2</td>
<td>63</td>
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<td>I/O</td>
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<tr>
<td>DVCC2</td>
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<td>I/O</td>
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<td>P8.5/TA1.0</td>
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<td>I/O</td>
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<td>P8.6/TA1.1</td>
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<td>I/O</td>
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<td>P8.7</td>
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<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P9.0/UCB2SSTE/UCB2CLK</td>
<td>68</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P9.1/UCB2SOMI/UCB2SCLA</td>
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<td>I/O</td>
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<tr>
<td>P9.2/UCB2SOMI/UCB2SCLB</td>
<td>70</td>
<td>N/A</td>
<td>I/O</td>
</tr>
</tbody>
</table>

Figure 228: MSP430F5438 - Pin description (3/5)[18]
## Appendix G (continued)

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P9.4/UC2TXD/UC2SIMO</td>
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<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P9.5/UC2RXD/UC2SOMI</td>
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<td>N/A</td>
<td>I/O</td>
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<td>P9.6</td>
<td>74</td>
<td>N/A</td>
<td>I/O</td>
</tr>
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<td>P9.7</td>
<td>75</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P10.0/UCB3STE/UC3CLK</td>
<td>76</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P10.1/UCB3SIMO/UCB3SDA</td>
<td>77</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P10.2/UCB3SOMI/UCB3SCL</td>
<td>78</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P10.3/UCB3CLK/UC3STE</td>
<td>79</td>
<td>N/A</td>
<td>I/O</td>
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<td>P10.4/UC3TXD/UC3SIMO</td>
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<td>I/O</td>
</tr>
<tr>
<td>P10.5/UC3RXD/UC3SOMI</td>
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<td>P10.6</td>
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<td>P10.7</td>
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<td>I/O</td>
</tr>
<tr>
<td>P11.0/ACLK</td>
<td>84</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P11.1/MCLK</td>
<td>85</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>P11.2/SMCLK</td>
<td>86</td>
<td>N/A</td>
<td>I/O</td>
</tr>
<tr>
<td>DVCC4</td>
<td>87</td>
<td>07</td>
<td>Digital power supply</td>
</tr>
<tr>
<td>DVSS4</td>
<td>88</td>
<td>08</td>
<td>Digital ground supply</td>
</tr>
<tr>
<td>P5.2/XT2IN</td>
<td>89</td>
<td>69</td>
<td>I/O</td>
</tr>
<tr>
<td>P5.3/XT2OUT</td>
<td>90</td>
<td>70</td>
<td>I/O</td>
</tr>
<tr>
<td>TEST/8WTCLOCK</td>
<td>91</td>
<td>71</td>
<td>I</td>
</tr>
<tr>
<td>PJ.0/TDO(4)</td>
<td>92</td>
<td>72</td>
<td>I/O</td>
</tr>
<tr>
<td>PJ.1/TDI/TCLK(4)</td>
<td>93</td>
<td>73</td>
<td>I/O</td>
</tr>
</tbody>
</table>

Figure 229: MSP430F5438 - Pin description (4/5)[18]
<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NO.</th>
<th>IO(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2/TMS(4)</td>
<td>94</td>
<td>74</td>
<td>I/O General-purpose digital I/O Test mode select</td>
</tr>
<tr>
<td>P2/TCK(4)</td>
<td>95</td>
<td>75</td>
<td>I/O General-purpose digital I/O Test clock</td>
</tr>
<tr>
<td>RST/NMI/SBWDIO(5)</td>
<td>96</td>
<td>76</td>
<td>I/O Reset input active low Non-maskable interrupt input Spy-bug wire data input/output</td>
</tr>
<tr>
<td>P0.0/A0</td>
<td>97</td>
<td>77</td>
<td>I/O General-purpose digital I/O Analog input A0 – ADC</td>
</tr>
<tr>
<td>P0.1/A1</td>
<td>98</td>
<td>78</td>
<td>I/O General-purpose digital I/O Analog input A1 – ADC</td>
</tr>
<tr>
<td>P0.2/A2</td>
<td>99</td>
<td>79</td>
<td>I/O General-purpose digital I/O Analog input A2 – ADC</td>
</tr>
<tr>
<td>P0.3/A3</td>
<td>100</td>
<td>80</td>
<td>I/O General-purpose digital I/O Analog input A3 – ADC</td>
</tr>
</tbody>
</table>

Figure 230: MSP430F5438 - Pin description (5/5)
Appendix H

GERBER FILES
Appendix H (continued)

Figure 231: PCB Layer 1 (Mentor Graphics environment)
Appendix H (continued)

Figure 232: PCB Layer 4 (Mentor Graphics environment)
Figure 233: PCB Layer 6 (Mentor Graphics environment)
Figure 234: PCB Solder-mask layer (Mentor Graphics environment)
Figure 235: PCB Solder-mask and silk-generator layer (Mentor Graphics environment)
Appendix I

SEQUENCE DIAGRAMS

Figure 236: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Figure 237: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Appendix I (continued)

Figure 238: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Appendix I (continued)

Figure 239: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Figure 240: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Figure 241: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Figure 242: Get PowerDCDC output voltage - sequence diagram (Visual Paradigm)
Appendix J

CC1020 - SOFTWARE OPERATIONS
Appendix J (continued)

The following routines allow to handle the transceiver in all its functions. All the register addresses are loaded into the UML description in order not to handle binary strings.

**Signature:** ReadReg(registro : ushort) : byte, Scope : classifier

**Signature:** SetReg(registro : byte, dato : byte) :

```c
void, Scope: classifier, Code Body: char count;

//*CONFIG_PORT_OUT = 0;
PSEL.write(false);
PCLK.write(false);
PDO.write(false);
PDI.write(false);
WAIT_CYCLE();
for (count = 6; count >= 0; count --)
{
    //*CONFIG_PORT_OUT = (((registro >> count) & 0x01) << PDI);
    PDI.write(((registro >> count) & 0x01);
    WAIT_CYCLE();
    //*CONFIG_PORT_OUT |= (1<<PCLK);
    PCLK.set();
    WAIT_CYCLE();
```

}
// *CONFIG_PORT_OUT &= ~(1 << PCLK);

PCLK.reset();
}

// write byte

// *CONFIG_PORT_OUT |= 1 << PDI;
PDI.set();
WAIT_CYCLE();

// *CONFIG_PORT_OUT |= (1 << PCLK);
PCLK.set();
WAIT_CYCLE();

// *CONFIG_PORT_OUT &= ~(1 << PCLK);
PCLK.reset();
WAIT_CYCLE();

for (count = 7; count >= 0; count --)
{

    // *CONFIG_PORT_OUT = (((dato >> count) & 0x01) << PDI);

    PDI.write(((dato >> count) & 0x01);

    WAIT_CYCLE();

    // *CONFIG_PORT_OUT |= (1 << PCLK);
PCLK.set();
WAIT_CYCLE();

//*CONFIG_PORT_OUT &= ~<<PCLK);
PCLK.reset();
}
WAIT_CYCLE();

//*CONFIG_PORT_OUT = (1<<PSEL);
PSEL.set();
WAIT_CYCLE();

Signature: WAIT_CYCLE(), Scope: classifier

Signature: SetFreqA(freq : ulong, clockDivider : byte)
: void, Scope: classifier, Code Body: long val =
(ulong)(2*32768*(freq/(Fxtal/clockDivider)-0.75)+0.5);
SetReg(CC1020_FREQ_2A,(char)(val>>16));
SetReg(CC1020_FREQ_1A,(char)((val>>8)&0xFF));
SetReg(CC1020_FREQ_0A,(char)(val&0xFF));

Signature: SetFreqB(freq : ulong, clockDivider : byte)
: void, Scope: classifier, Code Body: long val =
(ulong)(2*32768*(freq/(Fxtal/clockDivider)-0.75)+0.5);
SetReg(CC1020_FREQ_2B,(char)(val>>16));
Appendix J (continued)

SetReg(CC1020_FREQ_1B,(char)((val>>8)&0xFF));
SetReg(CC1020_FREQ_0B,(char)(val&0xFF));

Signature: AFC_Control(Settling : ushorts, Dev : ushorts):
    void , Scope: classifier, Code Body: const short RXdev_X
    = (short)(3*Dev)/(1<<5)*(Baud_rate));

const short RXdev_M = (short)((3*Dev*(1<<3))/(1<<RXdev_X)
    *(Baud_rate)));

SetReg(CC1020_AFC_CONTROL, (RXdev_M | (RXdev_X<<4) |
    (Settling <<6)));

Signature: Deviation(Tx_Shaping : ushorts, Dev : ushorts):
    void , Scope: classifier, Code Body: // float TXdev_M=(
    Dev*(2^(16-TXdev_X))/Fxtal); // float TXdev_M=(dev*
    (2^(16-TXdev_X)))/(Fxtal/2);// Fref?
    // while (((TXdev_M<8)||(TXdev_M>=16))&&(!Dev!=0))
    // {
    // if (TXdev_M<8)
    // TXdev_X=TXdev_X-1;
    // else
    // TXdev_X=TXdev_X+1;
Appendix J (continued)

// TXdev_M = (Dev*(2^(16-TXdev_X)))/(Fxtal);

const short TXdev_X = (short) floor((Dev*(1<<13))/
(Fxtal/ClockDivider));

const short TXdev_M = (short) ((Dev*((long)1<<16))/
((1<<TXdev_X)*Fxtal/ClockDivider));

SetReg(CCI020_DEVIATION, (TXdev_M | (TXdev_X<<4) |
(Tx_Shaping<<7)));

Signature: VGA3(VGA_Down : byte, VGA_Setting : byte) :
void, Scope: classifier, Code Body: SetReg(CCI020_VGA3,
(VGA_Setting | (VGA_Down<<5)));

Signature: VGA4(VGA_Up : byte, CS_Level : byte) : void,
Scope: classifier, Code Body: SetReg(CCI020_VGA4, (CS_Level
| (VGA_Up<<5)));

Signature: Lock(Lock_Select : byte, Window_Width : byte,
Lock_Mode : byte, Lock_Accuracy : byte) : void, Scope:
classifier, Code Body: SetReg(CCI020_LOCK,(Lock_Accuracy
| (Lock_Mode<<2) | (Window_Wdth<<3) | (Lock_Select<<4)));
Appendix J (continued)

Signature: Analog(Band_Select : byte, LO_DC : byte, PD_Long : byte, Div_Buff_Current : byte, PA_Boost : byte) : void,
    Scope: classifier, Code Body: byte VGA_Blanking = (AGC_Desable ==1 ? 1 : 0);
SetReg(CC1020_ANALOG,(Div_Buff_Current | (PA_Boost<<2) | (0<<3) | (PD_Long<<4) | (VGA_Blanking<<5) | (LO_DC<<6) | (Band_Select<<7)));
Signature: Buff_Swing(Pre_Swing : byte, RX_Swing : byte, TX_Swing : byte) : void, Scope: classifier, Code Body:
    SetReg(CC1020_BUFF_SWING,(TX_Swing | (RX_Swing<<3) | (Pre_Swing<<6)));
Signature: Buff_Current(Pre_Current : byte, RX_Current : byte, TX_Current : byte) : void, Scope: classifier,
    Code Body: SetReg(CC1020_BUFF_CURRENT,(TX_Current | (RX_Current<<3) | (Pre_Current<<6)));
Signature: Frontend(LNAmix_Current : byte, LNA_Current : byte, Mix_Current : byte, LNA2_Current : byte, SDC_Current : byte, LNAmix_Bias : byte) : void, Scope: classifier,
    Code Body: SetReg(CC1020_FRONTEND,(LNAmix_Bias | (SDC_Current<<1) | (LNA2_Current<<2) | (Mix_Current<<3)
    | (LNA_Current<<4) | (LNAmix_Current<<6)));
Signature: PA_Power(PA_High : byte, PA_Low : byte) :
void, Scope: classifier, Code Body: SetReg(CCI020_PA_POWER,
(PA_Low | (PA_High<<4)));

Signature: Match(RX_Match : byte, TX_Match : byte) :
void, Scope: classifier, Code Body: SetReg(CCI020_Match,
(TX_Match | (RX_Match<<4)));

Signature: Power_Down() : void, Scope: classifier,
Code Body: byte PD = (PD_Mode==2 ? 1 : 0);
SetReg(CCI020_POWERDOWN,(PD<<ADC_PD | (PD<<Filter_PD) |
(PD<<VGA_PD) | (PD<<LNAmix_PD) | (PD<<CHP_PD) |
(PD<<Buff_PD) | (PD<<VCO_PD) | (PD<<PA_PD)));

Signature: Calibrate(Cal_Start : byte, Cal_Dual : byte,
Cal_Wait : byte, Cal_Iterate : byte) : void, Scope: classifier,
Code Body: SetReg(CCI020_CALIBRATE,( Cal_Iterate | (0<<3) |
(Cal_Wait<<4) | (Cal_Dual<<6) | (Cal_Start<<7)));

Signature: VGA2(LNA2_Min : byte, LNA2_Max : byte, AGC_Desable :
byte, AGC_Hysteresis : byte, AGC_AVG : byte) : void, Scope:
classifier, Code Body: char LNA2_Setting = (VGA_Setting<10 ? 0 : 1);
SetReg(CCI020_VGA2, (AGC_AVG | (AGC_Hysteresis<<2) |
(AGC_Desable<<3) | (LNA2_Setting<<4) | (LNA2_Max<<6) |
(LNA2_Min<<7)));
Appendix J (continued)

Signature: CC1020_Init() : void, Scope: classifier, Code Body:

    CONFIG_PORT_OUT = (1<<CONFIG_PSEL);
    CONFIG_PORT_SEL &= ~(1<<CONFIG_PSEL) | (1<<CONFIG_PDI)
    | (1<<CONFIG_PCLK) | (1<<CONFIG_PDO));
    CONFIG_PORT_DIR |= (1<<CONFIG_PSEL) | (1<<CONFIG_PDI)
    | (1<<CONFIG_PCLK);
    CONFIG_PORT_DIR &= ~(1<<CONFIG_PDO);

Signature: CC1020_Config_Carrier() : void, Scope:

    classifier, Code Body: Reset();

SetReg(CC1020_MAIN,0x81);
SetReg(CC1020_INTERFACE,0x4F);
    //IMPORTANT: SEP_DI_DO = 1
SetReg(CC1020_RESET,0xFF);
SetReg(CC1020_SEQUENCING,0x8F);
    //SetReg(CC1020_FREQ_2A,0x3A);
    //SetReg(CC1020_FREQ_1A,0x7A);
    //SetReg(CC1020_FREQ_0A,0xF1);
SetFreqA (436.69271e6);
    //SetReg(CC1020_CLOCK_A,0x39);
Clock_A (2,6,1);
    //SetReg(CC1020_FREQ_2B,0x3A);
Appendix J (continued)

```c
// SetReg (CC1020_FREQ_1B, 0x85);
// SetReg (CC1020_FREQ_0B, 0x9D);
SetFreqB (437.00e6, 2);
// SetReg (CC1020_CLOCK_B, 0x39);
Clock_B(2,6,1);
SetReg(CC1020_VCO,0x44);
// SetReg (CC1039_MODEM, 0x50);
Modem(Fxtal /307200.0, 0, 1);
// SetReg (CC1020_DEVIATION, 0x00);
Deviation(0, 0.0);
// SetReg (CC1020_AFC_CONTROL, 0x3B);
AFC_Control(0, 35200);
// SetReg (CC1020_FILTER, 0x27);
FilterBandWidth(43000.0);
// SetReg (CC1020_VGA1, 0x61);
VGA1(1,1,0,1);
// SetReg (CC1020_VGA2, 0x55);
VGA2(0,1,0,1,1);
// SetReg (CC1020_VGA3, 0x13);
VGA3(0,19);
// SetReg (CC1020_VGA4, 0x17);
```
VGA4(0,23);
// SetReg (CC1020_LOCK, 0x20);
Lock(2,0,0,0);
// SetReg (CC1020_FRONTEND, 0x78);
Frontend(1,3,1,0,0,0);
// SetReg (CC1020_ANALOG, 0x47);
Analog(0,1,0,1,3);
// SetReg (CC1020_BUFF_SWING, 0x14);
Buff_Swing(0,2,4);
// SetReg (CC1020_BUFF_CURRENT, 0x22);
Buff_Current(0,4,2);
// SetReg (CC1020_PLL_BW, 0xAE);
PLL_BW();
// SetReg (CC1020_CALIBRATE, 0x34);
Calibrate(0,0,3,4);
// SetReg (CC1020_PA_POWER, 0xF0);
PA_Power(15,0);
// SetReg (CC1020_MATCH, 0x00);
Match(0,0);
SetReg(CC1020_PHASE_COMP, 0x00);
SetReg(CC1020_GAIN_COMP, 0x00);
Appendix J (continued)

```
// SetReg(CCI020_POWERDOWN, 0x00);

Power_Down();

SetReg(CCI020_TEST1, 0x4D);
SetReg(CCI020_TEST2, 0x10);
SetReg(CCI020_TEST3, 0x06);
SetReg(CCI020_TEST4, 0x00);
SetReg(CCI020_TEST5, 0x40);
SetReg(CCI020_TEST6, 0x00);
SetReg(CCI020_TEST7, 0x00);
return (ReadReg(CCI020_STATUS2));

Signature: Reset() : bool, Scope: classifier,

Code Body:

CC1020_SetReg(CCI020_MAIN, PD_MODE_1 | FS_PD | XOSC_PD | BIAS_PD);
CC1020_SetReg(CCI020_MAIN, PD_MODE_1 | FS_PD | XOSC_PD |
| BIAS_PD | RESET_N);

if ( CC1020_ReadReg(CCI020_FREQ_1A) == 0xB1 )
  return TRUE;
else
  return FALSE;
```
Signature: Clock_A(clockDivider : byte, MCLK_DIV1 : byte, MCLK_DIV2 : byte) : void, Scope: classifier,
Code Body: SetReg(CC1020_CLOCK_A, (MCLK_DIV2 | MCLK_DIV1<<2 | ((clockDivider -1)<<5)));

Signature: Clock_A(clockDivider : byte, baud : ulong) : void, Scope: classifier, Code Body: static const float x = Fxtal / clockDivider/8/64/baud;
static const byte MCLK_DIV1 = (x<=1.0? 0 : ((x<=2.0)? 1 : ((x<=4.0)? 2 : 3)));
static const float y = (x<=1? 1.0 : (x<=2)? 2.0 :
(x<=4)? 4.0 : 8.0);
static const float z = x / y;
static const byte MCLK_DIV2 = (z<=2.0? 0 : ((x<=3.0)? 1 :
((x<=4.0)? 2 : ((x<=8.0)? 3 : ((x<=12.0)? 4 : ((x<=25.0)? 5 : ((x<=40.0)? 6 : 7))))));

SetReg(0x1, (MCLK_DIV2 | MCLK_DIV1<<2 |
(((clockDivider -1)<<5)));

Signature: Clock_B(clockDivider : byte, MCLK_DIV1

Appendix J (continued)

: byte, MCLK_DIV2 : byte) : void, Scope: classifier,

Code Body: SetReg(CCI020_CLOCK_B, (MCLK_DIV2 | MCLK_DIV1<<2 | ((clockDivider -1)<<5));

Signature: Modem(ADC_F : ulong, scrambling : byte,

Data_Format : byte) : void, Scope: classifier,

Code Body: // float ADC_Fr_Ideal=4*FI;

// long ADC_Fr=Fxtal/ADC_Fr_Ideal;

const ushort ADC_Fr = (ushort)(ADC_F /4);

int ADC_Div;

if (ADC_Fr<=5)
ADC_Div = 1<<4;
else if (ADC_Fr<=7)
ADC_Div = 2<<4;
else if (ADC_Fr<=9)
ADC_Div = 3<<4;
else if (ADC_Fr<=11)
ADC_Div = 4<<4;
else if (ADC_Fr<=13)
ADC_Div = 5<<4;
else if (ADC_Fr<=15)
ADC_Div = 6<<4;
else

ADC_Div = 7<<4;

SetReg(CCI020_MODEM, ((Data_Format−1) |
(scrambling<<2) | (0<<3) | ADC_Div | (0<<7)));

Signature: FilterBandWidth(bw : ulong, baud : ulong)
: void, Scope: classifier, Code Body:

    byte FILTER_BYPASS = (baud>=76800 ? 1<<7 : 0);

byte DEC_DIV = (byte)(307200.0/bw);

//byte DEC_SHIFT = (DEC_DIV<=1 ? 0 :
(DEC_DIV<=24 ? 1<< : 2<<));

byte DEC_SHIFT;

if (bw>=307200.0/1)
    DEC_SHIFT = 0;
else if (bw>=307200.0/24)
    DEC_SHIFT = 1<<5;
else
    DEC_SHIFT = 2<<5;

SetReg(CCI020_FILTER, (DEC_DIV | DEC_SHIFT
| FILTER_BYPASS));

Signature: VGA1(CS_Set : byte , CS_Reset : byte ,
Appendix J (continued)

VGA_Wait : byte, VGA_Freeze : byte) : void,

Scope: classifier, Code Body: //byte VGA_Wait

= (180e-6 <= 209 ? 0 : 1);

SetReg(CC1020_VGA1, (VGA_Freeze | (VGA_Wait << 2)

| (CS_Reset << 5) | (CS_Set << 6)));
Appendix K

INPUT/OUTPUT DRIVER - OPERATIONS
Appendix K (continued)

It is the driver for generic I/O pins of microcontroller. Each pin must be instantiated by setting the template parameters as:

- **port**: address of register corresponding to the output port associated with the desired pin;
- **bit**: mask corresponding to the specific bit of output port associated with the desired pin;
- **invert**: sets the logic levels of the signal connected (True when the high-logic level stands for active, false the other way round).

Signature: `init() : void`, Scope: classifier,

Code Body: `input();
interruptEnable(false);
interruptEdgeSelect(false);
clearInterruptFlag();`

Signature: `input() : void`, Scope: classifier,

Code Body: `(* (volatile byte *) (PORT + DELTA_DIR)) &= ~BIT;`

Signature: `output() : void`, Scope: classifier,

Code Body: `(* (volatile byte *) (PORT + DELTA_DIR)) |= BIT;`

Signature: `read() : bool`, Scope: classifier,

Code Body: `if (INVERT) {
    if ((* (volatile byte *) (PORT + DELTA_IN)))`
& BIT) return false; else return true;
}

} else {
    if ((volatile byte *) (PORT + DELTA_IN)) & BIT) return true; else return false;
}

Signature: write(val : bool) : void, Scope: classifier, Code Body: if (INVERT) {
    if (val)
        (*PORT) &= ~BIT;
    else
        (*PORT) | = BIT;
} else {
    if (val)
        (*PORT) | = BIT;
    else
        (*PORT) & = ~BIT;
}

Signature: set() : void, Scope: classifier,
Code Body: if (INVERT) {

Appendix K (continued)

(*PORT) & = ¬BIT;
}
else {

(*PORT) |= BIT;
}

Signature: reset() : void, Scope: classifier,
Code Body: if (INVERT) {

(*PORT) |= BIT;
}
else {

(*PORT) & = ¬BIT;
}

Signature: interruptEnable(on : bool) : void,
Scope: classifier, Code Body: if (on)

(* (volatile byte *) (PORT + DELTA_IE)) |=

BIT;
else

(* (volatile byte *) (PORT + DELTA_IE)) & =

¬BIT;

Signature: interruptEdgeSelect(rising : bool)
: void, Scope: classifier, Code Body: if (rising)
Appendix K (continued)

(* (volatile byte *) (PORT + DELTA_IE)) &= ~BIT;

else

(* (volatile byte *) (PORT + DELTA_IE)) |= BIT;

Signature: setPressingEdge() : void, Scope:

classifier, Code Body: if (INVERT)

interruptEdgeSelect(false);

else

interruptEdgeSelect(true);

Signature: setReleaseEdge() : void, Scope:

classifier, Code Body: if (INVERT)

interruptEdgeSelect(true);

else

interruptEdgeSelect(false);

Signature: clearInterruptFlag() : void, Scope:

classifier, Code Body: (* (volatile byte *)

(PORT + DELTA_IFG)) &= ~BIT;

Signature: getInterruptFlag() : bool, Scope:

classifier, Code Body: return (bool)
Appendix K (continued)

\(((* (volatile byte *) (PORT + DELTA_IFG)) & BIT)\);
Appendix L

PROCESSOR/UARTA0 (UARTB2) - OPERATIONS
Appendix L (continued)

The following code allows to initialize the MSP430F5438A within the MSP430m family.

Signature: Processor(), Scope: instance,

Code Body: init();

Signature: init() : void, Scope: classifier,

Code Body: #if MSP430x43x

// configures FLL
SCFI0 = 0; // set clock divide to 1 in FLL
// configures SMCLK = DCO/1; the other
clocks are irrelevant
FLL_CTL0 |= DCOPLUS;

// configures XTAL2 to off; SMCLK on;
MCLK = DCO; SMCLK = DCO
FLL_CTL1 &= ~(SMCLKOFF | XT2OFF | SELM0
    | SELMI | SELS | FLL_DIV0 | FLL_DIV1);
FLL_CTL1 |= XT2OFF;

//setDCO(CALBC1_8MHZ, CALDCO_8MHZ);
clock.setACLK(MSP430::XT1CLK, 1);
clock.setMCLK(MSP430::XT1CLK, 1);
clock.setSMCLK(MSP430::XT1CLK, 1);
clock.resetFlags();
IE1 &= ~OFIE;
IFG1 &= ~OFIFG;

#elif MSP430x24x

BCSCTL2 = 0*SELM0 | 0*DIVM0 | 0*SELS |
0*DIVS0 | 0*DOOR;
BCSCTL3 = 0*XT2S0 | 0*LFXT1S0 | 0*XCAP0;
clock.setDCO(CALBCI_8MHZ, CALDCO_8MHZ);
clock.setACLK(MSP430::XT1CLK, 1);
clock.setMCLK(MSP430::XT1CLK, 1);
clock.setSMCLK(MSP430::XT1CLK, 1);
resetFlags();
IE1 &= ~OFIE;
IFG1 &= ~OFIFG;

#elif MSP430x54x

UCSCTL6 = 0*XT2DRIVE0 + 0*XT2BYPASS +
XT2OFF + 0*XT1DRIVE0 + 0*XTS + 0*XT1BYPASS +
0*XCAP0 + SMCLKOFF + XT1OFF;
clock.setACLK(XT1CLK, 1);
clock.setMCLK(XT1CLK, 1);
clock.setSMCLK(XT1CLK, 1);
clock.resetFlags();
Appendix L (continued)

SFRIE1 &= ¬OFIE;
SFRIFG1 &= ¬OFIFG;

#else
    warning unsupported processor
#endif

Signature: setLPM(mode : t_LPModes) : void,
Scope: classifier

The following code refers to the UARTA0 interface. However, all the routines are valid
for the UARTB2 interface just by changing the corresponding identifier (B2 instead of A0).
Registers are different, but functions are equivalent.

Signature: init(mode : t_UART_MODES, baud_rate : ushort) : void, Scope: classifier, Code Body:

    // #ifdef MSP430x43x / MSP430x24x || MSP430x54x
    (see tagged value "header")
    // ctl  ->  U0CTL / UCA0CTL0
    // ctl_1 ->  / UCA0CTL1
    // tctl  ->  U0TCTL
    // br0  ->  U0BR0 / UCA0BR0
    // br1  ->  U0BR1 / UCA0BR1
Appendix L (continued)

// mctl -> UOCTL / UCA0MCTL
// irctl -> UCA0IRCTL
// irrctl -> UCA0IRRCTL
// stat -> UCA0STAT
// abctl -> UCA0ABCTL

UCA0br0 = (byte) (CLOCK_FREQ / baud_rate);
    // baud rate
UCA0br1 = (byte) (((short)(CLOCK_FREQ /
    baud_rate)) >> 8); // baud rate

#if MSP430x43x

switch (mode) {

case SPI_MASTER_MODE:

    ctl = CHAR | SYNC | SWRT | MM;    //
    sets USART0 for 8–bit, synchronous, SPI mode, Master

tctl = SSEL1 | STC;        //
    sets USART0 for:

    // clock polarity (writes on
    rising edge; reads on falling edge),
// clock phase (clock=0 when inactive)

// 3-wire mode

// SMCLK clock (master clock)
br0 = (byte) (CLOCK_FREQ / baud_rate);
    // baud rate

br1 = (byte) (((short)(CLOCK_FREQ / baud_rate)) >> 8); // baud rate

mctl = 0x00;
    // must be 0 in SPI mode

break;

case SPI_SLAVE_MODE:

    ctl = CHAR | SYNC | SWRST;
    // sets USART0 for 8-bit, synchronous,

    SPI mode, Slave

tctl = 0;
    // sets USART0 for:

    // clock polarity (writes on rising edge; reads on falling edge),

    // clock phase (clock=0 when inactive)

    // 4-wire mode
### Appendix L (continued)

```c
// UCLK clock (for slave)
br0 = 0x00;

// baud rate (0 for slave)
br1 = 0x00;

// baud rate (0 for slave)
mctl = 0x00;

// must be 0 in SPI mode
break;

case RS232_MODE:

    // TBD!

c    = CHAR | SYNC | SWRST | MM;

    // sets USART0 for 8-bit, synchronous, SPI mode, Master
break;

case I2C_MASTER_MODE:

    break;

case I2C_SLAVE_MODE:

    break;

case IRDA_MODE:

    break;

}

ME1 &= !USPIE0;
```
Appendix L (continued)

// Module disable

ctl &= ~SWRST;

// SW reset of UART

#if elif MSP430x24x || MSP430x54x

if ((mode == SPI_MASTER_MODE)
|| (mode == SPI_SLAVE_MODE)) {

UCA0ctl_1 = UCSSEL1 | UCSSEL0 // clock from SMCLK

| 0*UCRXEIE // erroneous characters rejected

| 0*UCBRKIE // break characters

set interrupt flag

| 0*UCDORM // not dormant;

all characters are received

| 0*UCTXADDR // all frames are data; no address

| 0*UCTXBRK // frames are not break

| UCSWRST; // SW reset

UCA0ctl_0 = 0*UCCKPH // writes on

first (rising) edge of UCLK; reads on second (falling) edge

| 0*UCCKPL // clock polarity (active high)
Appendix L (continued)

| 0*UCMSB // LSB first
| 0*UC7BIT // eight bits
| UCMST // master
| 0*UCMODE1 | 0*UCMODE0 // 3-pin SPI mode
| UCSYNC; // synchronous mode

UCA0br0 = (byte) (CLOCK_FREQ /
 baud_rate);               // baud rate
UCA0br0 = (byte) (((short)(CLOCK_FREQ
 / baud_rate)) >> 8); // baud rate
UCA0mctl = UCOS16; // Oversampling
 mode; temporarily disabled modulation TBD

} // if ((mode == I2C_MASTER_MODE)

|| (mode == I2C_SLAVE_MODE)) {
  // NOT IMPLEMENTED in UART A0
  // }

if ((mode == SPI_SLAVE_MODE)
  || (mode == I2C_SLAVE_MODE)) {
  UCA0ctl_0 &= ~UCMST; // slave
}
if ((mode == RS232_MODE) ||
(mode == IRDA_MODE)) {

UCA0ctl_1 = UCSSEL1 | UCSSEL0

// clock from SMCLK
| 0*UCRXEIE // erroneous characters rejected
| 0*UCBRKIE // break characters
reset interrupt flag
| 0*UCDORM // not dormant;
all characters are received
| 0*UCTXADDR // all frames are data; no address
| 0*UCTXBRK // frames are not break
| UCSWRS; // SW reset
UCA0ctl_0 = UCPEN // parity enabled
| 0*UCPAR // odd parity
| 0*UCMSB // LSB first
| 0*UC7BIT // eight bits
| 0*UCSPB // one stop bit
| 0; // UART mode
Appendix L (continued)

UCA0br0 = (byte) (CLOCK_FREQ / baud_rate / 16);
    // baud rate
UCA0br1 = (byte) (((short)
    (CLOCK_FREQ / baud_rate / 16)) >> 8);
    // baud rate
UCA0mctl = UCOS16; // Oversampling
    mode; temporarily disabled modulation TBD
if ((mode == IRDA_MODE)) {
    UCA0irtctl = (((PULSE_WIDTH *
    (CLOCK_FREQ / 1000)) / 1000000) &
    0x3F) << 2) // pulse width for IrDA mode
        | UCIIRTXCLK // IrDA pulse clock
          select (TBD)
        | UCIIREN; // enable IrDA encoder/decoder
   UCA0irrcctl = (((PULSE_WIDTH/2 * (CLOCK_FREQ /
    1000)) / 1000000) & 0x3F) << 2) // pulse
    width for IrDA mode
        | 0*UCIRRXPL // IrDA pulse is positive
        | UCIIRXF; // enable IrDA receiver filter
}
 Appendix L (continued)

```c
{
UCA0stat = 0; // clear all status bits
UCA0abctl = 0; // disable auto baudrate detector
UCA0ctl_1 &= ~UCSWRST; // remove SW reset

#else

warning unsupported_processor

#endif

disable(mode);
// Module disable

Signature: init(mode : t_UART_MODES) :
void, Scope: classifier, Code Body:

return init(mode, BAUD_RATE);

Signature: msbFirst() : void, Scope:
classifier, Code Body: #if MSP430x43x
ctl_1 |= UCSWRST; // set SW reset
```
Appendix L (continued)

```c
ctl_0 |= UCMSB; // MSB first
ctl_1 &= ~UCSWRST; // remove SW reset
#endif

#if MSP430x24x || MSP430x54x
    UCA0ctl_1 |= UCSWRST; // set SW reset
    UCA0ctl_0 |= UCMSB; // MSB first
    UCA0ctl_1 &= ~UCSWRST; // remove SW reset
#endif

Signature: enable(mode : t_UART_Modes) :

void, Scope: classifier, Code Body: #if MSP430x43x
    ctl |= SWRST; // resets the UART, therefore clears TX and RX buffers
#endif

if ((mode == SPI_MASTER_MODE) || (mode == SPI_SLAVE_MODE)) {
    P3SEL |= (BIT1 | BIT2 | BIT3);
    // P3.1,2,3 set as normal input pins (MOSI, MISO, SCK)
}
// if ((mode == I2C_MASTER_MODE)
```
Appendix L (continued)

|| (mode == I2C_SLAVE_MODE)) {
    // NOT IMPLEMENTED in UART A0
    // }

if ((mode == RS232_MODE) || (mode == IRDA_MODE)) {
    P3SEL |= (BIT1 | BIT2);
    // P3.1,2,3 set as normal input pins (MOSI, MISO, SCK)
}
ME1 |= USPIE0;
// Module enable
cntl &= ~SWRST;
#endif

#ifif MSP430x24x || MSP430x54x
    UCA0ctl_1 |= UCSWRT; // SW reset
    if ((mode == SPI_MASTER_MODE) || (mode == SPI_SLAVE_MODE)) {
        P3SEL |= (BIT4 | BIT5 | BIT0);
        // UART pins set for UART usage
    }
}
Appendix L (continued)

// if ((mode == I2C_MASTER_MODE) || (mode == I2C_SLAVE_MODE)) {
// NOT IMPLEMENTED in UART A0
// }

if ((mode == RS232_MODE) || (mode == IRDA_MODE)) {
    P3SEL |= (BIT4 | BIT5); // UART pins set for UART usage
}
UCA0ctl_1 &= ~UCSWRST; // SW reset
#endif

Signature: disable(mode : t_UART_MODES):

: void, Scope: classifier, Code Body:

    enableInterrupts (false, false);

#if MSP430x43x

    c1 |= SWRST;
    // resets the UART, therefore clears TX and RX buffers
    ME1 &= ~USPIE0;
#endif
Appendix L (continued)

    // Module disable

if ((mode == SPI_MASTER_MODE) ||
    (mode == SPI_SLAVE_MODE)) {
  P3SEL &= ~(BIT1 | BIT2 | BIT3);
    // P3.1,2,3 set as normal inputs
  P3DIR &= ~(BIT1 | BIT2 | BIT3);
    // P3.1,2,3 set as normal inputs
}

    // if ((mode == I2C_MASTER_MODE)
|| (mode == I2C_SLAVE_MODE)) {
    // NOT IMPLEMENTED in UART A0
    // }

if ((mode == RS232_MODE) ||
    (mode == IRDA_MODE)) {
  P3SEL &= ~(BIT1 | BIT2);
    // P3.1,2,3 set as normal inputs
  P3DIR &= ~(BIT1 | BIT2);
    // P3.1,2,3 set as normal inputs
}

ctl &= ~SWRST;
Appendix L (continued)

```c
#define

#if MSP430x24x || MSP430x54x

UCA0ctl_1 |= UCSWST; // SW reset
UCA0ctl_1 &= ~UCSWST; // SW reset

if (((mode == SPI_MASTER_MODE) ||
    (mode == SPI_SLAVE_MODE)) {

    P3SEL &= ~(BIT4 | BIT5 | BIT0);
    // UART pins set for normal usage
    P3DIR &= ~(BIT4 | BIT5 | BIT0);
    // UART pins set as normal inputs
}

// if ((mode == I2C_MASTER_MODE)
|| (mode == I2C_SLAVE_MODE)) {
// NOT IMPLEMENTED in UART A0
// }

if (((mode == RS232_MODE) || (mode ==
IRDA_MODE)) {

    P3SEL &= ~(BIT4 | BIT5); // UART pins
    set for normal usage
```
Appendix L (continued)

P3DIR &= ~(BIT4 | BIT5);  // UART pins

set as normal inputs

}

#endif

Signature: enableInterrupts(enTXinterrupt : bool, enRXinterrupt : bool) : void, Scope: classifier,

Code Body: #if MSP430x43x

if (enTXinterrupt) {

    IE1 |= UTXIE0;  // enables TX interrupt

}

else {

    IE1 &= ~UTXIE0;  // disables TX interrupt

}

if (enRXinterrupt) {

    IE1 |= URXIE0;  // enables RX interrupt

}

else {

    IE1 &= ~URXIE0;  // disables RX interrupt

}
 Appendix L (continued)

}  
#endif

#if MSP430x24x

if (enTXinterrupt) {
    IE2 |= UCA0TXIE;  // enables TX interrupt
}
else {

    IE2 &= ~UCA0TXIE;  // disables TX interrupt
}
#if MSP430x54x

if (enRXinterrupt) {
    IE2 |= UCA0RXIE;  // enables RX interrupt
}
else {

    IE2 &= ~UCA0RXIE;  // disables RX interrupt
}
#endif
if (enTXinterrupt) {
    UCA0ie |= UCTXIE; // enables TX interrupt
}
else {
    UCA0ie &= ~UCTXIE; // disables TX interrupt
}
if (enRXinterrupt) {
    UCA0ie |= UCRXIE; // enables RX interrupt
}
else {
    UCA0ie &= ~UCRXIE; // disables RX interrupt
}
#endif

Signature: writeData(data : byte) : void, Scope: classifier, Code Body: // TX buffer has short lifetime, therefore it is not hardened!

#ifdef MSP430x43x
Appendix L (continued)

U0TXBUF = data;

#define

#if MSP430x24x || MSP430x54x
UCA0TXBUF = data;
#endif

Signature: writeData(data : byte, CRC : byte) :

    void, Scope: classifier, Code Body: writeData(data);
CRC ^= data;

Signature: writeData(data : byte, CRC : TripleByte) :

    void, Scope: classifier, Code Body: writeData(data);
CRC ^= data;

Signature: readData() : byte, Scope: classifier,
Code Body: // RX buffer is volatile, therefore it
is not hardened!

#if MSP430x43x
return U0RXBUF;

Appendix L (continued)

```c
#if MSP430x24x || MSP430x54x
    return UCA0RXBUF;
#endif

Signature: readData(CRC : byte) : byte, Scope: classifier, Code Body: byte tmp;
    tmp = readData();
    CRC ^= tmp;
    return tmp;

Signature: readData(CRC : TripleByte) : byte,
    Scope: classifier, Code Body: byte tmp;
    tmp = readData();
    CRC ^= tmp;
    return tmp;

Signature: isTXready() : bool, Scope: classifier,
    Code Body: // interrupt flags are volatile,
    therefore they are not hardened!
```
Appendix L (continued)

```c
#define MSP430x43x

    return ((IFG1 & UTXIFG0) == UTXIFG0);
#endif

#define MSP430x24x

    return ((IFG2 & UCA0TXIFG) == UCA0TXIFG);
#endif

#define MSP430x54x

    return ((UCA0IFG & UCTXIFG) == UCTXIFG);
#endif

Signature: isTXempty() : bool, Scope: classifier,

Code Body:  // status flags are volatile,

    therefore they are not hardened!

#define MSP430x43x

    return ((U0TCTL & TXEPT) == TXEPT);
#endif

#define MSP430x24x  ||  MSP430x54x
```
Appendix L (continued)

```c
return ((UCA0STAT & UCBUSY) == 0);
#endif

Signature: isRXready() : bool, Scope: classifier,
Code Body: // status flags are volatile,
therefore they are not hardened!

#if MSP430x43x
return ((IFG1 & URXIFG0) == URXIFG0);
#endif

#if MSP430x24x
return ((IFG2 & UCA0RXIFG) == UCA0RXIFG);
#endif

#if MSP430x54x
return ((UCA0IFG & UCRXIFG) == UCRXIFG);
#endif

Signature: RX() : pin, Scope: classifier
Signature: TX() : pin, Scope: classifier
Signature: MISO() : pin, Scope: classifier

Signature: MOSI() : pin, Scope: classifier

Signature: SCK() : pin, Scope: classifier

Signature: refresh() : void, Scope: classifier,

Code Body: 

```c
#if defined(HARDENED)
UCA0ctl_0.refresh();
UCA0ctl_1.refresh();
UCA0br0.refresh();
UCA0br1.refresh();
UCA0mctl.refresh();
UCA0irtctl.refresh();
UCA0irrctl.refresh();
UCA0stat.refresh();
UCA0abctl.refresh();
UCA0ie.refresh();
#endif
```
Appendix M

ADC/FLASH MEMORY - OPERATIONS
Appendix M (continued)

The following code allows to handle the analog-to-digital converters which are integrated in the microcontroller.

Signature: init(sampletime : ushort, Vref :
t_ADC_VREF, channels : ushort) : void, Scope:
classifier, Code Body: const int temp =

sampletime * (CLOCK_FREQ >> 20); // divide

by approx 1e6

ushort sampletime_int = 0;

if (temp < 6)

    sampletime_int = 0; // 4 cycles

else if (temp < 12)

    sampletime_int = 1; // 8 cycles

else if (temp < 24)

    sampletime_int = 2; // 16 cycles

else if (temp < 48)

    sampletime_int = 3; // 32 cycles

else if (temp < 80)

    sampletime_int = 4; // 64 cycles

else if (temp < 112)

    sampletime_int = 5; // 96 cycles
else if (temp < 160)
    sampletime_int = 6; // 128 cycles
else if (temp < 224)
    sampletime_int = 7; // 192 cycles
else if (temp < 320)
    sampletime_int = 8; // 256 cycles
else if (temp < 448)
    sampletime_int = 9; // 384 cycles
else if (temp < 640)
    sampletime_int = 10; // 512 cycles
else if (temp < 896)
    sampletime_int = 11; // 768 cycles
else
    sampletime_int = 12; // 1024 cycles

#if MSP430x43x || MSP430x24x
    adc12ctl0 &= ~ADC12ENC; // ADC disabled,
    otherwise no other parameter can be changed !!!
    // Sets ADC12ENC = 0 to enable ADC configuration
    adc12ctl0 = (SHT00 + SHT10) * sampletime_int |
    // defines duration of sample phase
Appendix M (continued)

0*ADC12MSC | // single conversion
0*ADC12ON | // turns off ADC
0*ADC12TOVIE | // no interrupt enabled
0*ADC12OVIE | // no interrupt enabled
0*ADC12ENC | // ADC disabled
0*ADC12SC; // don’t start conversion

adc12mctl0 = 0*INCH0 | 0*ADC12REFON;
// selects input channel 0

switch (Vref) {
    case VREF_EXT:
        adc12mctl0 |= SREF2 | SREF1 | SREF0;
        break;
    case VREF_1_25:
        adc12mctl0 |= 0*SREF2 | 0*SREF1 | SREF0;
        adc12ctl0 |= 0*ADC12REF2_5V; //
        sets internal reference to 2.5V
        break;
    case VREF_2_5:
Appendix M (continued)

adc12mctl0 |= 0*SRF2 | 0*SRF1 | SRF0;
adc12ctl0 |= ADC12REF2_5V;

// sets internal reference to 2.5V
break;
case VREF_VDD:
    adc12mctl0 |= 0*SRF2 | 0*SRF1 | 0*SRF0;
    break;
}

adc12ctl1 = CSTARTADD0 * 0 |

// selects conversion to location ADC12MEM0
0*SHS0 | // selects start from SW
SHP |

// selects sample from timer
ADC12DIV0 * (int)(clock_freq/CLOCK_MAX)
| // selects fastest clock
ADC12SSEL0 | ADC12SSEL1 |
// selects clock from SMCLK
0*CONSEQ0;

// selects single acquisition
### Appendix M (continued)

```c
adc12ie = 0;
ADC12IFG = 0;
ADC12IV = 0;

P6SEL |= channels & 0xFF;
P6DIR &= ~(channels & 0xFF);
P5SEL |= ((channels >> 8) & 0x10) >> 3;
P5SEL |= ((channels >> 8) & 0x20) >> 5;
P5DIR &= ~(((channels >> 8) & 0x10) >> 3);
P5DIR &= ~(((channels >> 8) & 0x20) >> 5);
P4SEL |= ((channels >> 8) & 0x40) << 1;
P4SEL |= ((channels >> 8) & 0x80) >> 1;
P4DIR &= ~(((channels >> 8) & 0x40) << 1);
P4DIR &= ~(((channels >> 8) & 0x80) >> 1);

#if MSP430x54x
adc12c10 &= ~ADC12ENC; // ADC disabled, otherwise no other parameter can be changed !!!
#endif
// Sets ENC = 0 to enable ADC configuration
adc12c10 = (ADC12SHT00 + ADC12SHT10) *
```
Appendix M (continued)

sampleTime_int | // defines duration of sample phase
0*ADC12MSC | // single conversion
0*ADC12ON | // turns on ADC
0*ADC12TOVIE | // no interrupt enabled
0*ADC12OVIE | // no interrupt enabled
0*ADC12ENC | // ADC disabled
0*ADC12SC; // don't start conversion

adc12mct10 = 0* ADC12INCH0 | 0*ADC12REFON;
// selects input channel 0

switch (Vref) {
    case VREF_EXT:
        adc12mct10 | = ADC12SREF2 | ADC12SREF1
        | ADC12SREF0;
        break;
    case VREF_1_25:
        adc12mct10 | = 0*ADC12SREF2 |
        0*ADC12SREF1 | ADC12SREF0;
        adc12ct10 | = 0*ADC12REF2_5V;
Appendix M (continued)

// sets internal reference to 2.5V
break;

case VREF_2_5:
    adc12mctl0 |= 0*ADC12SREF2 |
    0*ADC12SREF1 | ADC12SREF0;
    adc12ctl0 |= ADC12REF2_5V;
    // sets internal reference to 2.5V
    break;

case VREF_VDD:
    adc12mctl0 |= 0*ADC12SREF2 |
    0*ADC12SREF1 | 0*ADC12SREF0;
    break;
}

adc12ctl1 = ADC12CSTARTADD0 * 0 |
// selects conversion to location ADC12MEM0
0*ADC12SHS0 |
// selects start from SW
ADC12SHP |
// selects sample from timer
ADC12DIV0 * (int)(CLOCK_FREQ/
Appendix M (continued)

// selects fastest clock
ADC12SEL0 | ADC12SEL1 |
// selects clock from SMCLK
0*ADC12CONSEQ0;
// selects single acquisition

adcl2ctl2 = 0*ADC12PDIV | // Predivide by 1
ADC12TCOFF | // Temperature sensor turned off
ADC12RES1 | ADC12RES0 * 0 | // 12 bit resolution
0*ADC12DF | // Data format:

unsigned binary (CA2), left align
ADC12SR | // Sampling
rate up to 50ksps
0*ADC12REFOUT | // Reference output on
0*ADC12REFBURST; //

Reference buffer on only during S&H

if (sampletime < 20)

adcl2ctl2 &^= ^ADC12SR; //
Sampling rate up to 50ksps

if (channels & 0x200)
Appendix M (continued)

```c
adc12ctl12 &= ~ADC12TCOFF; //

if temperature channel is enabled, enables temperature sensor

adc12ie = 0;
ADC12IFG = 0;
ADC12IV = 0;

P6SEL |= channels & 0xFF;
P6DIR &= ~(channels & 0xFF);
P7SEL |= (channels >> 8) & 0xF0;
P7DIR &= ~((channels >> 8) & 0xF0);

#else
warning unsupported processor
#endif

Signature: enable() : void , Scope:
classifier , Code Body: #if MSP430x43x
|| MSP430x24x || MSP430x54x

adc12ctl10 |=
    ADC12ON | // turns on ADC
```
Appendix M (continued)

0 * ADC12ENC | // ADC conversion

not enabled, otherwise no other parameter can be changed !!!

ADC12REFON; // enables internal reference to 2.5V

#endif

Signature: disable() : void, Scope:
classifier, Code Body: #if MSP430x43x
|| MSP430x24x || MSP430x54x
adc12ctl0 &= ~
ADC12ON | // turns on ADC
ADC12ENC | // ADC enabled
ADC12REFON ); // enables internal reference to 2.5V

#endif

Signature: select(channel : byte) :

void, Scope: classifier, Code Body:

#if MSP430x43x || MSP430x24x || MSP430x54x
adc12ctl0 &= ~ADC12ENC; //
Appendix M (continued)

ADC disabled, otherwise no other parameter can be changed !!!

#endif

#if MSP430x43x || MSP430x24x

adc12mctl0 & = ~(INCH0 * 0xF); // selects input channel
adc12mctl0 |= EOS | // end of sequence of acquisition
    INCH0 * (channel & 0xF); // selects input channel
#endif

#if MSP430x54x

adc12mctl0 & = ~(ADC12INCH0 * 0xF); // selects input channel
adc12mctl0 |= ADC12EOS | // end of sequence of acquisition
    ADC12INCH0 * (channel & 0xF); // selects input channel
#endif

#if MSP430x43x || MSP430x24x || MSP430x54x
adc12ctl0 |= ADC12ENC; // ADC disabled, otherwise no other parameter can be changed !!!

#ifend

Signature: start() : void, Scope:

classifier, Code Body: #if MSP430x43x

|| MSP430x54x

adc12ctl0 |= ADC12ENC | ADC12SC ;

// starts conversion

#endif

#if if MSP430x24x

adc12ctl0 |= ENC | ADC12SC ;

// starts conversion

#endif

Signature: isReady() : bool, Scope:

classifier, Code Body: #if MSP430x43x

|| MSP430x24x || MSP430x54x

return (adc12ctl1.read() & ADC12BUSY?
false : true );
Appendix M (continued)

```c
#define

Signature: read() : ush ort , Scope: classifier , Code Body: #if MSP430x43x || MSP430x24x || MSP430x54x

return (ush ort) ADC12MEM0;
#endif

Signature: convert() : ush ort , Scope: classifier , Code Body: start();

for (ush ort i=0; i<TIMEOUT; i++) {
    if (isReady()) break;
}

return read();

Signature: enableInterrupt() : void,

Scope: classifier , Code Body: #if

MSP430x43x || MSP430x24x || MSP430x54x
adc12ctl0 &= ~ADC12ENC; // ADC disabled,

otherwise no other parameter can be changed !!!
ADC12IFG &= ~BIT0; // Clears interrupt
```
Appendix M (continued)

flags for ADC12MEM0

adc12ie | = BIT0; // Enables interrupt on
writing ADC12MEM0

adc12ctl0 | = ADC12ENC; // ADC disabled, otherwise no other parameter can be changed !!!
#endif

Signature: disableInterrupt() : void, Scope:

classifier, Code Body: #if MSP430x43x ||

MSP430x24x || MSP430x54x

adc12ctl0 & = ~ADC12ENC; // ADC disabled,
otherwise no other parameter can be changed !!!
adc12ie & = 0x01; // Enables interrupt on
writing ADC12MEM0

ADC12IFG & = 0x01; // Clears interrupt

flags for ADC12MEM0

adc12ctl0 | = ADC12ENC; // ADC disabled, otherwise no other parameter can be changed !!!
#endif

Signature: isr_adc12() : void, Scope:
classifier, Code Body: // Reads value and stores into user-defined address

*value_ptr = read();

clearInterrupt();
Signature: acquire(channel: byte, value: ushort): void, Scope: classifier, Code Body:

value_ptr = &value; // stores address where to store data after acquisition

select(channel);
enableInterrupt();
start();

Signature: clearInterrupt(): void, Scope:
classifier, Code Body: #if MSP430x43x || MSP430x24x || MSP430x54x
// Clearing isr_adc12() interrupt flag
ADC12IFG = 0; // 8 individual flags
#endif
Appendix M (continued)

The following code allows to handle the flash memory which is integrated in the microcontroller.

Signature: init() : void, Scope: classifier

Signature: erase(bank : t_FLASH_BANK, segment : byte) : bool, Scope: classifier, Code Body:

FCTL3 = FKEY;  // Clear LOCK
FCTL3 = FKEY | (FCTL3 & 0xFF);  // clear LockA
wdt = WDTCIL & 0xFF;  // Store WDT status
WDTCIL = WDJFW | WDTIHD;  // Stop WDT

switch (bank) {
    case MASS:
        FCTL1 = FKEY | MERAS | ERASE;
        *BSL_A_first = 0;
        while (FCTL3 & BUSY) ;
        break;
    case BSL_A:
    case BSL_B:
    case BSL_C:
    case BSL_D:
    case BSL:
        FCTL1 = FKEY | ERASE;
switch (bank) {
    case BSL_A:
        *BSL_A_first = 0;
        break;
    case BSL_B:
        *BSL_B_first = 0;
        break;
    case BSL_C:
        *BSL_C_first = 0;
        break;
    case BSL_D:
        *BSL_D_first = 0;
        break;
    case BSL:
        *BSL_A_first = 0;
        while (FCTL3 & BUSY) ;
        FCTL1 = FKEY | ERASE;
        *BSL_B_first = 0;
        while (FCTL3 & BUSY) ;
        FCTL1 = FKEY | ERASE;
        *BSL_C_first = 0;
while (FCTL3 & BUSY) ;
FCTL1 = FWKEY | ERASE;
* BSL_D_first = 0;
break;
}
while (FCTL3 & BUSY) ;
break;
case INFO_A:
case INFO_B:
case INFO_C:
case INFO_D:
case INFO:

FCTL1 = FWKEY | ERASE;
switch (bank) {
case INFO_A:
    * INFO_A_first = 0;
    break;
case INFO_B:
    * INFO_B_first = 0;
    break;
case INFO_C:
null
Appendix M (continued)

case MAIN_B_seg:

case MAIN_C_seg:

case MAIN_D_seg:
segment &= (SEGMENT_LENGTH - 1);
FCTL1 = FWEKEY | ERASE;
switch (bank) {

case MAIN_A_seg:
    * (MAIN_A_first + SEGMENT_LENGTH * segment) = 0;
    break;

case MAIN_B_seg:
    * (MAIN_B_first + SEGMENT_LENGTH * segment) = 0;
    break;

case MAIN_C_seg:
    * (MAIN_C_first + SEGMENT_LENGTH * segment) = 0;
    break;

case MAIN_D_seg:
    * (MAIN_D_first + SEGMENT_LENGTH * segment) = 0;
    break;
}
while (FCTL3 & BUSY) ;
break;
case MAIN_A:

case MAIN_B:

case MAIN_C:

case MAIN_D:

case MAIN:

FCTL1 = FWKEY | MERAS;

switch (bank) {

case MAIN_A:
  * MAIN_A_first = 0;
  break;

case MAIN_B:
  * MAIN_B_first = 0;
  break;

case MAIN_C:
  * MAIN_C_first = 0;
  break;

case MAIN_D:
  * MAIN_D_first = 0;
  break;

case MAIN:
  * MAIN_A_first = 0;
while (FCTL3 & BUSY) ;
FCTL1 = FWKEY | MEREAS;
* MAIN_B_first = 0;
while (FCTL3 & BUSY) ;
FCTL1 = FWKEY | MEREAS;
* MAIN_C_first = 0;
while (FCTL3 & BUSY) ;
FCTL1 = FWKEY | MEREAS;
* MAIN_D_first = 0;
break;
}

while (FCTL3 & BUSY) ;
break;
}

WDTCTL = WDJPW | WDTCNTCL | wdt; // Re-enable WDT?
FCTL3 = FWKEY|LOCK; // Set LOCK
return ((FCTL3 & ACCVIFG) ? false : true);

Signature: lock() : void, Scope: classifier,
Code Body: FCTL1 = FWKEY; // Done. Clear WRT
FCTL3 = FWKEY | LOCK; // Set LOCK
Signature: initiateWrite() : void, Scope:
classifier, Code Body: wdt = WDTCTL & 0xFF;

   // Store WDT status
WDTCTL = WDTPW | WDTHOLD; // Stop WDT
FCTL3 = FWKEY; // Clear LOCK
FCTL1 = FWKEY | WRT; // Enable write

Signature: terminateWrite() : void, Scope:
classifier, Code Body: FCTL1 = FWKEY; // Done. Clear WRT
FCTL3 = FWKEY | LOCK; // Set LOCK
WDTCTL = WDTPW | WDTCLK | wdt; // Re-enable WDT

Signature: write(address : byte, data : byte)
   : void, Scope: classifier, Code Body: FCTL3 = FWKEY; // Clear LOCK
FCTL1 = FWKEY | WRT; // Enable write
*address = data; // writing into flash
FCTL1 = FWKEY; // Done. Clear WRT
FCTL3 = FWKEY | LOCK; // Set LOCK
Appendix M (continued)

Signature: read(address : byte, data : byte)

: byte, Scope: classifier, Code Body: return

*address; // reading from flash
CITED LITERATURE


21. Datasheets - RF6886. RFMD.

22. Datasheets - CXE-2089Z. RFMD.

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